

# K470SDR Development Platform

user's manual

**Rev. 1.0**

Revision History

| Edition | Revision Date | Revisions            |
|---------|---------------|----------------------|
| 1.0     | July 7, 2026  | V1.0 Initial Version |
|         |               |                      |
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# Catalogue

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## 1 Introduction to the Development Board

The RFEVM development board consists of an RFSOM core board and a carrier board, with the two boards connected via a high-speed board-to-board connector.

The RFSOM core board employs the Xilinx Zynq™ UltraScale+™ RFSoc Gen3 series ZU47 DR FPGA as its main chip. This chip supports eight 14-bit RF-ADCs with a maximum sampling rate of up to 5 GSPS, and eight 14-bit RF-DACs with a maximum sampling rate of up to 9.84 GSPS. It reduces the complexity of the RF signal processing chain, maximizes the density of input/output channels without compromising bandwidth, leverages heterogeneous processing capabilities, and achieves lower power consumption by eliminating ADC/DAC components and removing the power consumption associated with FPGA-to-analog interfaces. The Zynq UltraScale+ family offers an ARM Cortex-A53 processing subsystem, UltraScale+ programmable logic, and high signal processing bandwidth, enabling the implementation of integrated RF signal chains that meet the requirements of wireless communications, cable TV access, test and measurement, early warning/radar systems, and other high-performance RF applications.

The carrier board extends the core board with a wide array of peripheral interfaces, including one M.2 SSD interface, one USB 3.0 interface, one Gigabit Ethernet interface, one JTAG/UART interface, one TF card interface, one SFP interface, and one QSFP interface.

The figure below shows a schematic diagram of the overall development system:

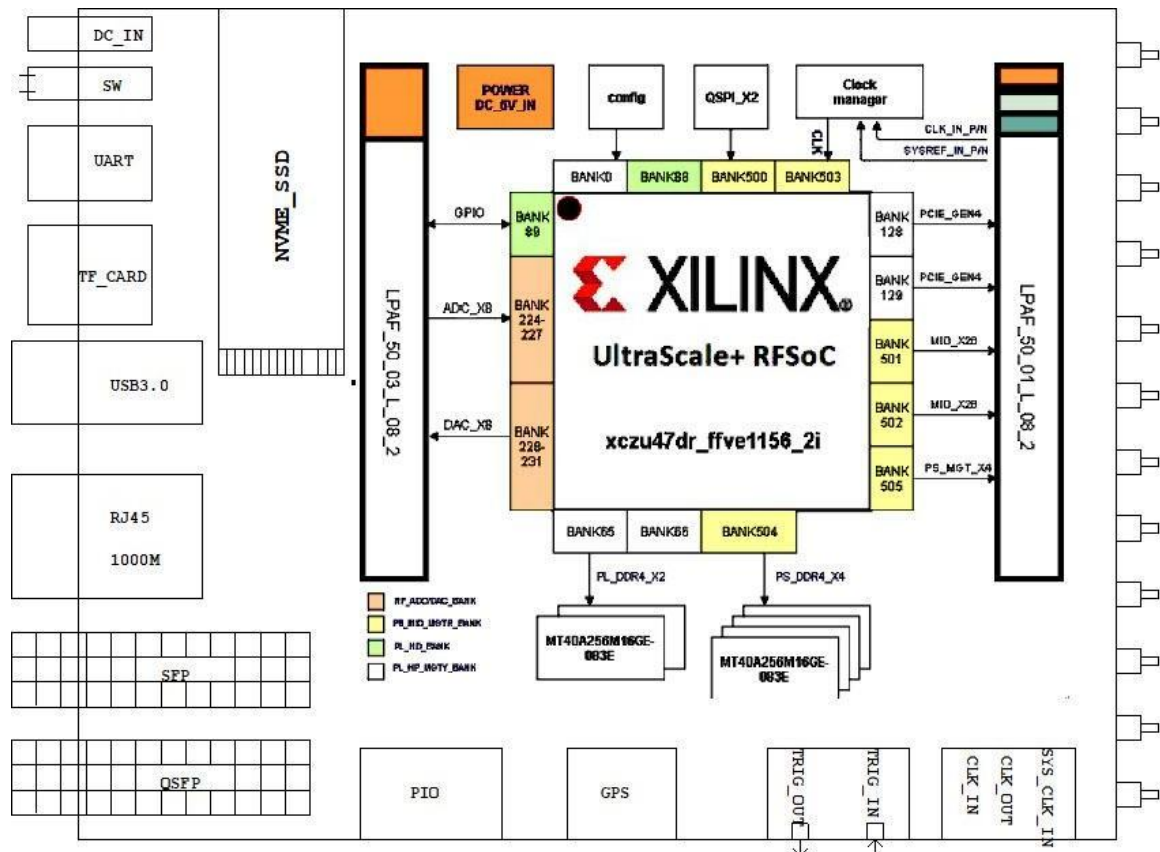


Figure 1: RFEVM development Board

From this schematic diagram, we can see the interfaces and functionalities available in the RFEVM development platform.

### ● RFSOM Core Board

The system consists of ZU47DR + 4 GB DDR4 (PS) + 2 GB DDR4 (PL) + 1 GB QSPI Flash; additionally, the core module provides dual crystal oscillator clock sources—one single-ended 33.3333 MHz active crystal oscillator for the PS system, and one 32.76 MHz crystal oscillator to drive the internal RTC circuit of the RFSOC.

### ● M.2 interface

A single PCIe x2 standard M.2 interface for connecting M.2 SSDs.

### ● USB 3.0 interface

Equipped with a USB 3.0 port along the entire length, supporting three operating modes: HOST, SLAVE, and others.

### ● Gigabit Ethernet interface

Equipped with 10M/100M/1000M Ethernet RJ45 ports for Ethernet data communication with computers or other network devices.

### ● JTAG & UART interfaces

The JTAG & UART debugging interface uses a Type-C interface, which is shared by both JTAG and UART.

For downloading and debugging FPGA programs.

- Micro SD card slot

A Micro SD card slot for storing the operating system image and the file system.

- QSFP28 fiber optic interface

Equipped with a QSFP28 fiber optic interface, it supports communication rates of 40G/100G.

- SFP fiber optic interface

Equipped with SFP interfaces along the entire path, supporting a communication rate of 10 Gbps.

- expandIO

There are three sets of extended I/O: two sets on the PL side and one set on the PS side, which can be customized by the user.

- LEDlamp

4 A scalable LED through-hole socket, allowing users to customize its use.

- key

A reset button.

## 2 RFSOM Core Board

### 2.1 Brief Introduction

The ZYNQ chip on the RFSOM core board is based on XILINX's Zynq™ UltraScale+™ RFSoc Gen3 series ZU47DR-2FFVE1156I.

This motherboard employs six DDR4 chips (MT40A512M16) from Micron Technology: four DDR4 chips are mounted on the PS side to form a 64-bit data bus width, while two DDR4 chips are mounted on the PL side to form a 32-bit data bus width. Each DDR4 chip has a capacity of 1 GB. The DDR4 SDRAM supports a maximum operating frequency of 1200 MHz (data rate of 2400 Mbps). Additionally, the motherboard integrates a 1 Gbit QSPI flash memory for boot storage, configuration, and system files.

To interface with the baseboard, the two 400-pin board-to-board connectors of this core board have been extended to include PS-side USB 3.0 interfaces, a Gigabit Ethernet interface, an SD card interface, an M.2 interface, and the remaining MIO interfaces; additionally, four pairs of PS MGT high-speed transceiver interfaces have been added; on the PL side, one QSFP 28 interface, one SFP interface, and the remaining IO interfaces have also been provided.



Figure 2: Front View of the RFSOM Core Board

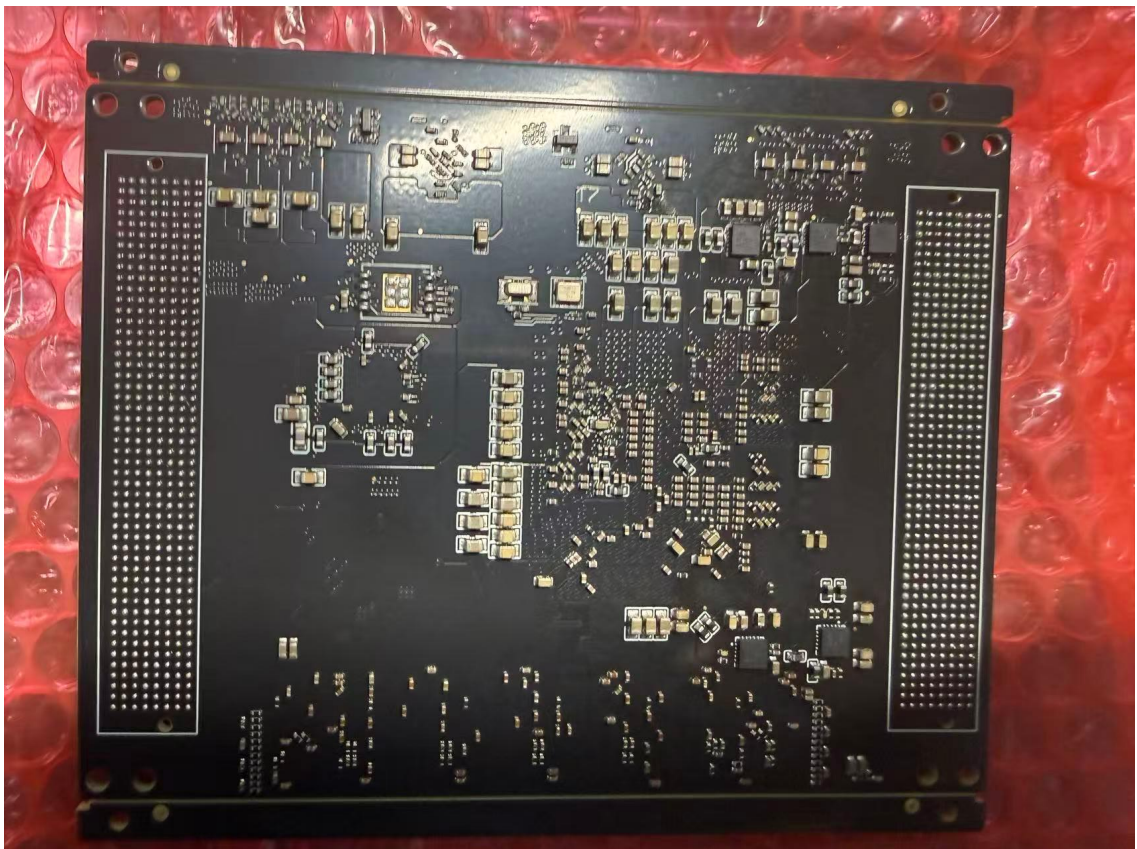


Figure 3: Back Side of the RFSOM Core Board

## 2.2 ZYNQ Chip

The RFSOM core board utilizes chips from Xilinx's Zynq™ UltraScale+™ RFSoc Gen3 series, specifically the ZU47DR-2FFVE1156I model. The FPGA resources within its programmable logic section provide high-throughput digital signal processing (DSP) capabilities and IP cores, such as digital up/down conversion (DUC/DDC) cores. By leveraging software-defined radio development, developers can easily integrate application programming interfaces (APIs) with the FPGA infrastructure to achieve FPGA acceleration. This approach enables rapid deployment and operation, allowing engineers to focus on value-added IP development. An FPGA system featuring commonly used functions—such as fast Fourier transform (FFT) and finite impulse response (FIR) filtering—serves as an excellent starting point. Subsequently, developers can incorporate their own IP blocks into a modular architecture using their preferred hardware description language (HDL). In addition to its system FPGA architecture, the Xilinx UltraScale+ RFSoc features four onboard application processing units (APUs) and two real-time processing units (RPU), making it suitable for applications requiring onboard embedded operating systems for independent operation.

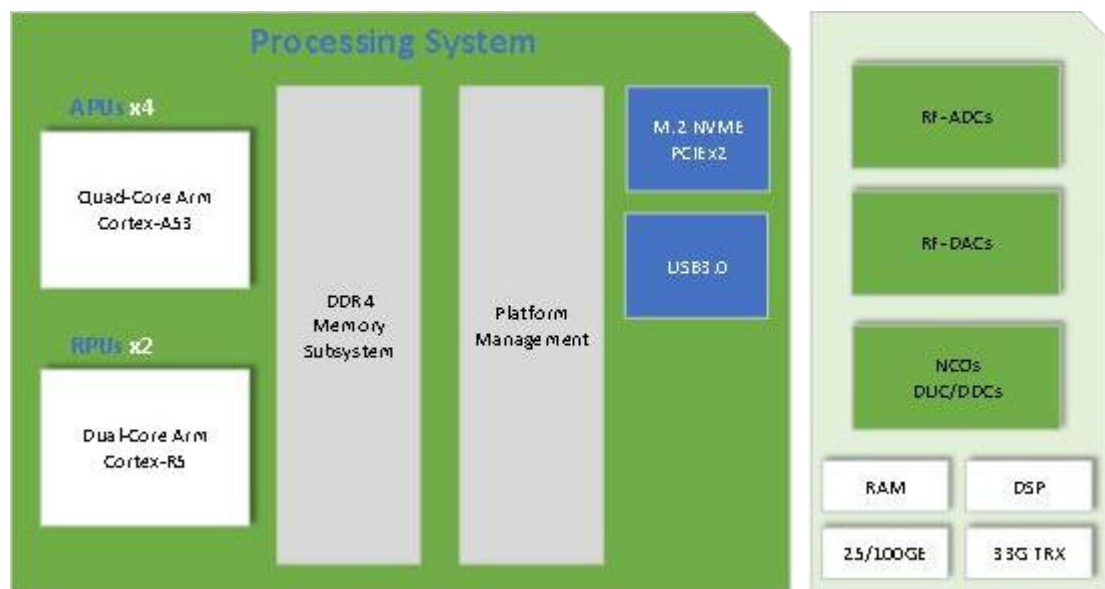


Figure 4: Block Diagram of the RFSOM Hardware System

RFSOM supports full-differential extraction of AD/DA channels; users can configure an RF conditioning circuit according to their requirements, with support for DC and AC coupling, as well as conditioning circuits for PA and LNA amplifiers. Additionally, it supports optional RF front-ends, including LO frequency converters, duplexers, PAs, and LNAs.

### 2.3 DDR4 SDRAM

The RFSOM core board is equipped with six 1 GB DDR4 chips from Micron (model MT40A512M16GE-083E), of which four DDR4 chips are mounted on the PS side, providing a 64-bit data bus bandwidth, and two DDR4 chips are mounted on the PL side, providing a 32-bit data bus bandwidth. The DDR4 SDRAM on the PS side supports a maximum operating frequency of 1200 MHz (data rate of 2400 Mbps), and the four DDR4 chips form a direct memory module.

It is connected to the memory interface of the BANK504 on the PS side. The DDR SDRAM on the PL side supports a maximum operating speed of 1200 MHz (data rate: 2400 Mbps), and two DDR4 modules are connected to the interfaces of BANK65 and BANK66 on the FPGA. The specific configurations of the DDR4 SDRAM on the PS and PL sides are shown in the following table. Table 1 DDR4 SDRAM Configuration

| Position | Item            | Chip model         | Capacity  | Vender |
|----------|-----------------|--------------------|-----------|--------|
| PS       | UM5,UM6,UM7,UM8 | MT40A512M16GE-083E | 512x16bit | Micron |
| PL       | UM1,UM2         | MT40A512M16GE-083E | 512x16bit | Micron |

The hardware connection scheme for DDR4 on the PS side is shown in the figure below:

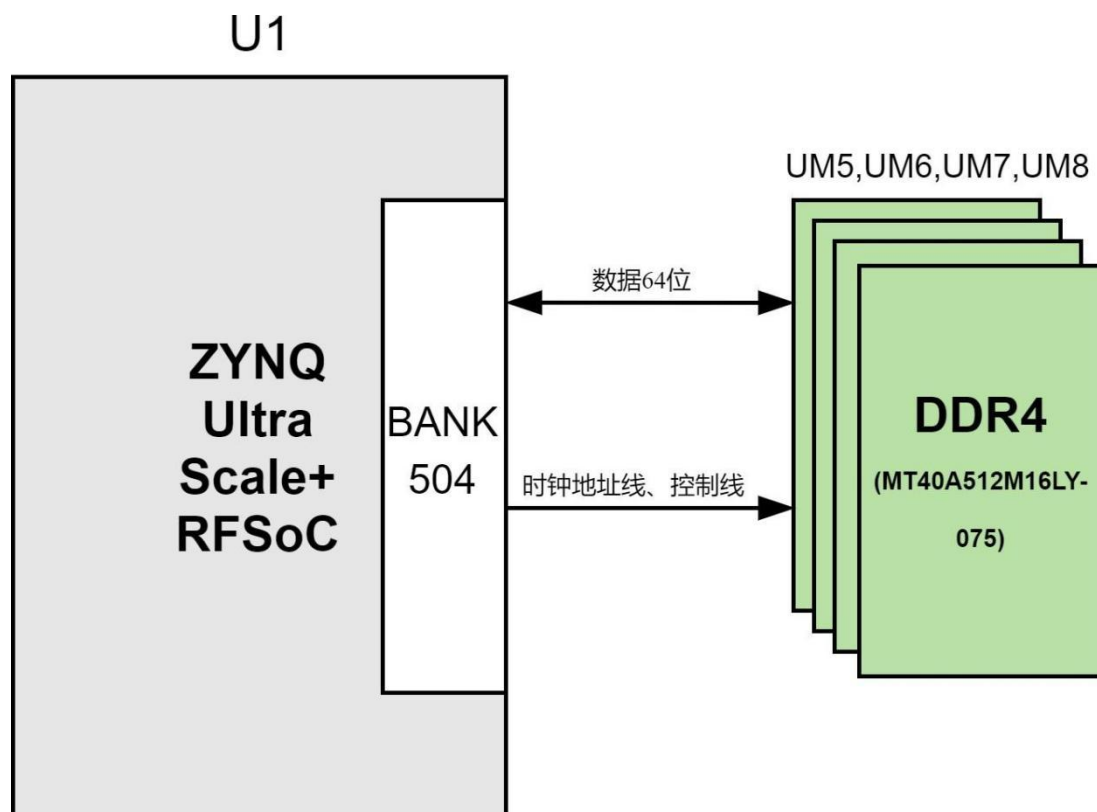


Figure 5: PS-Side DDR4 SDRAM connection Schematic

The hardware connection scheme for the DDR4 SDRAM on the PL side is shown in the figure below:

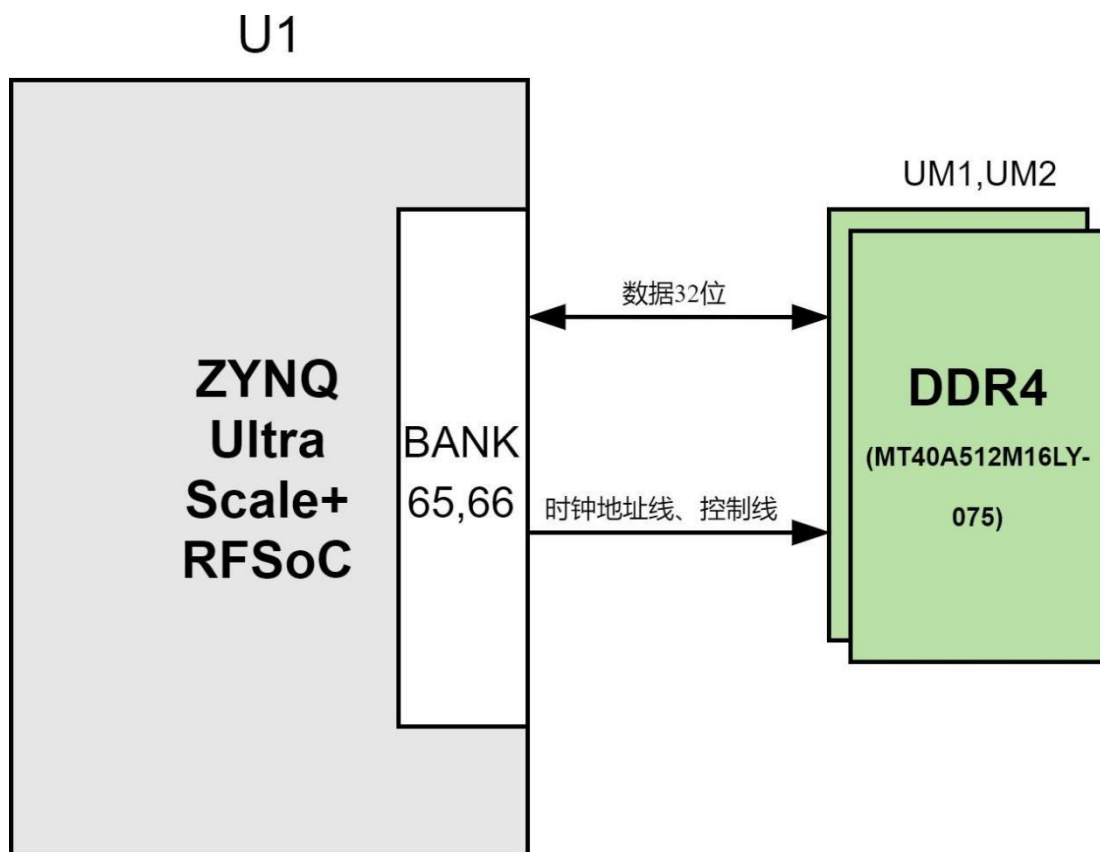


Figure 6: PL-Side DDR4 SDRAM connection Schematic

## 2.4 QSPI FLASH

The RFSOM core board is equipped with two 512 Mbit QUAD SPI FLASH chips that together form an 8-bit bandwidth data bus; the FLASH chip model is MT25QU512ABBIW9-0SIT, which operates under a 1.8 V CMOS voltage standard. Due to the non-volatility of the QSPI FLASH, it can serve as the system boot device to store the system boot image during operation. These images primarily consist of bit files for the FPGA, ARM application code, and its user data files. For specific QSPI FLASH models and their corresponding characteristics, refer to the table below.

Table 2: QSPI FLASH Models and Parameters

| Position | Item  | Chip model           | Capacity | Vender          |
|----------|-------|----------------------|----------|-----------------|
| PS       | U5,U6 | MT25QU512ABBIW9-0SIT | 512M bit | Magnesium light |

The QSPI FLASH is connected to the MIO pins of BANK500 in the PS section of the ZYNQ chip; in system design, these PS-side MIO pins must be configured to support the QSPI FLASH interface.

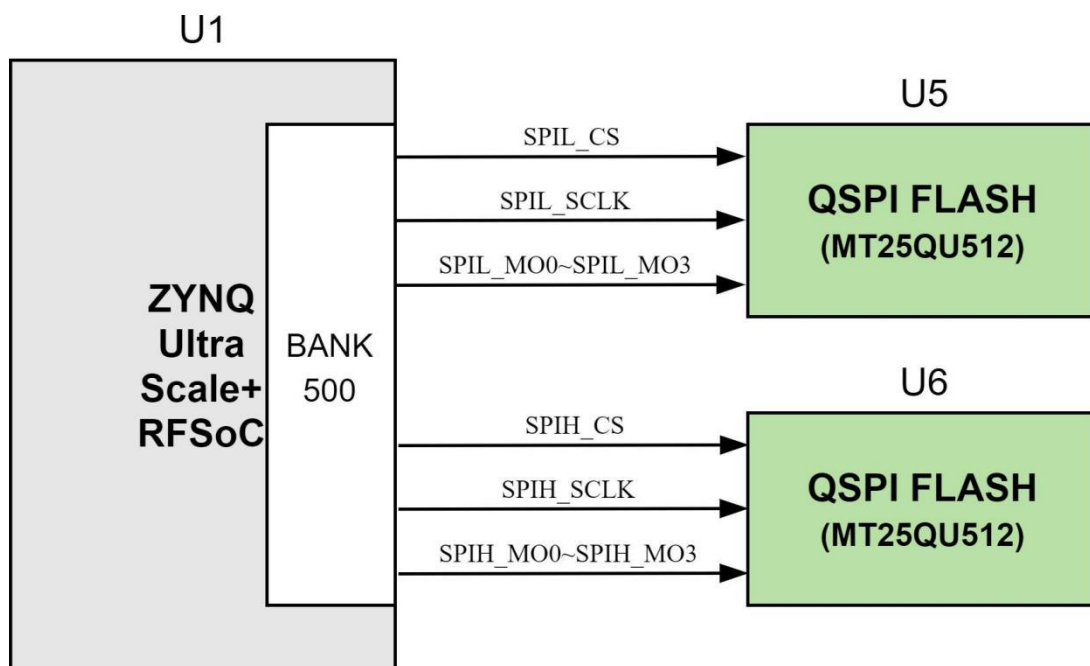


Figure 7: Schematic Diagram of QSPI FLASH Connection

Table 3 Shows the Chip Pin Assignment Configuration.

| Signal Name | Pin Name | Pin Number |
|-------------|----------|------------|
| SPII_SCLK   | PS_MIO0  | J17        |
| SPII_MO1    | PS_MIO1  | J18        |
| SPII_MO2    | PS_MIO2  | J16        |
| SPII_MO3    | PS_MIO3  | K16        |
| SPII_MO0    | PS_MIO4  | G15        |
| SPII_CS     | PS_MIO5  | H18        |
| SPIH_CS     | PS_MIO7  | K17        |
| SPIH_MO0    | PS_MIO8  | E15        |
| SPIH_MO1    | PS_MIO9  | F15        |
| SPIH_MO2    | PS_MIO10 | C15        |
| SPIH_MO3    | PS_MIO11 | G16        |
| SPIH_SCLK   | PS_MIO12 | B15        |

## 2.5 EEPROM

The RFSOM core module features an onboard EEPROM, model AT24CM01, with a capacity of 1 Mbit, which communicates with the PS end via an I2C bus.

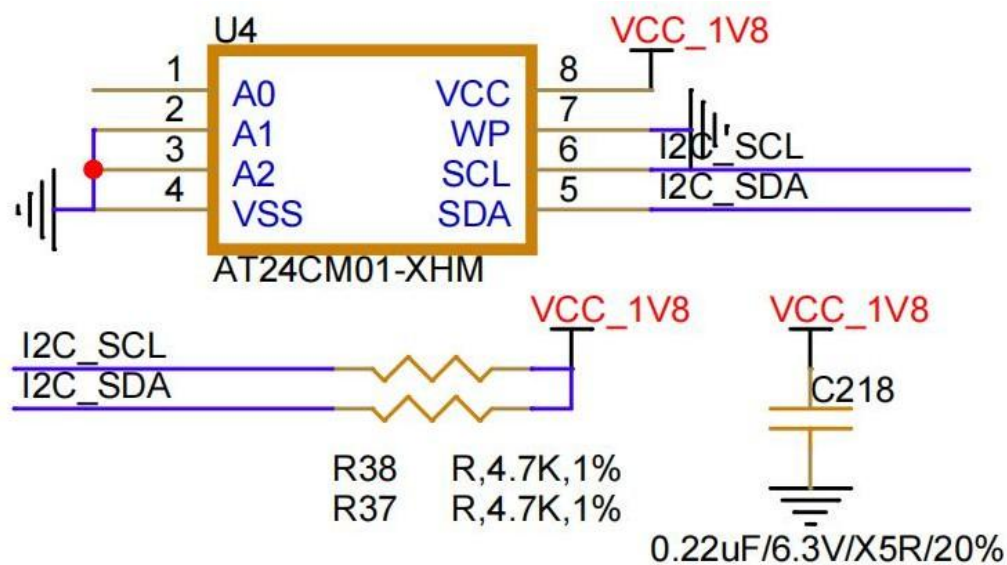


Figure 8: EEPROM Hardware Schematic

Table 4: EEPROM Pin Assignment

| Signal Name | Pin Name | Pin Number | Remarks          |
|-------------|----------|------------|------------------|
| IIC_SDA     | PS_MIO25 | B17        | I2C data signal  |
| IIC_SCL     | PS_MIO24 | A17        | I2C clock signal |

## 2.6 Clock Configuration

The core module provides dual crystal oscillator clocks; the system clock defaults to a 33.3333 MHz active crystal oscillator, housed in a  $3.2 \times 2.5$  mm package. A 32.768 kHz crystal oscillator drives the internal RTC circuit of the RFSOC. A schematic diagram of the clock circuit design is shown in the figure below:

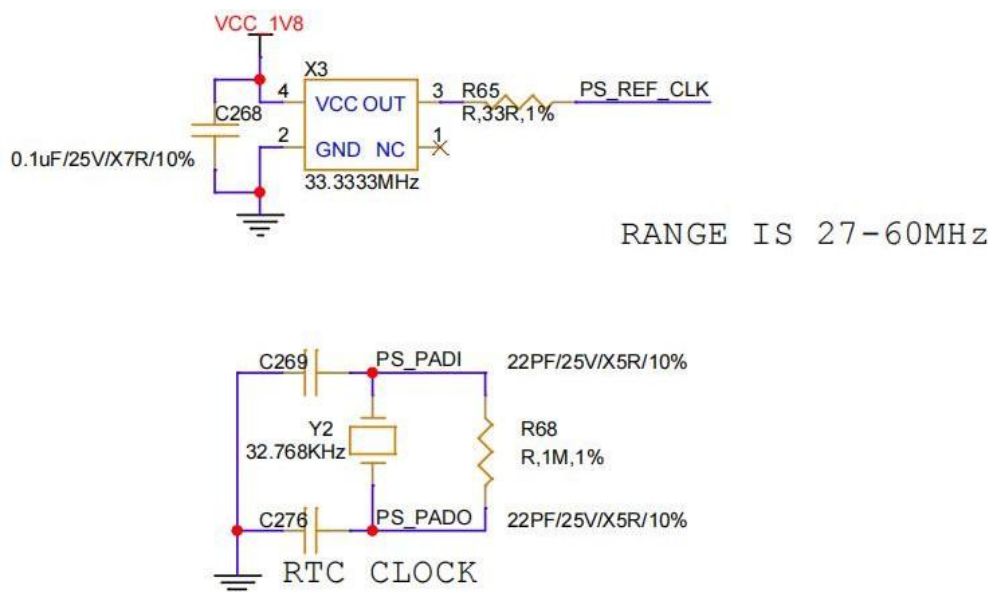


Figure 9 Schematic Diagram of the Crystal Oscillator

The core module system employs the LMK04828 clock chip to allocate the required clocks for each module, utilizing a 19.2 MHz high-stability OCXO as the master oscillator. It supports GTY recovery clock functionality, allows the input of external reference clocks alongside the SYSREF input, and enables multiple modules to be connected in parallel to form larger-scale phase-locked RF channels.

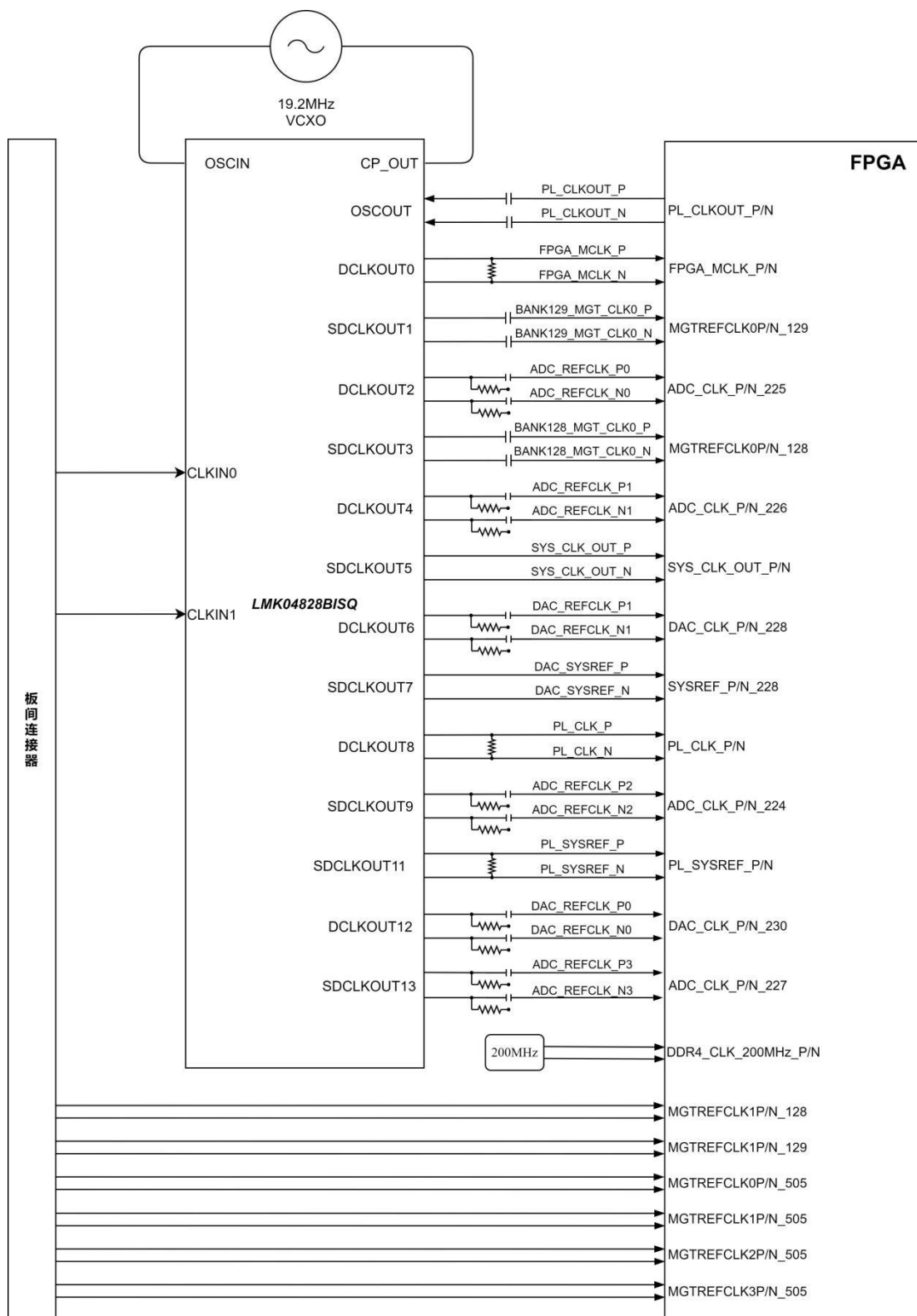


Figure 10 Schematic Diagram of Clock Distribution Connections

## 2.7 PS-GTR Interfaces

The PS-side GTR high-speed BANK of the RFSOM core module is not utilized at all; instead, it is entirely routed via connectors. It supports data rates up to 6.0 Gb/s and can be used as an x1, x2, or x4 interface in PCIe Gen2.

It can also be used as a SATA drive, supporting data rates of 1.5 Gb/s, 3.0 Gb/s, and 6 Gb/s, and can also support DP interfaces, USB 3.0 interfaces, and other applications.

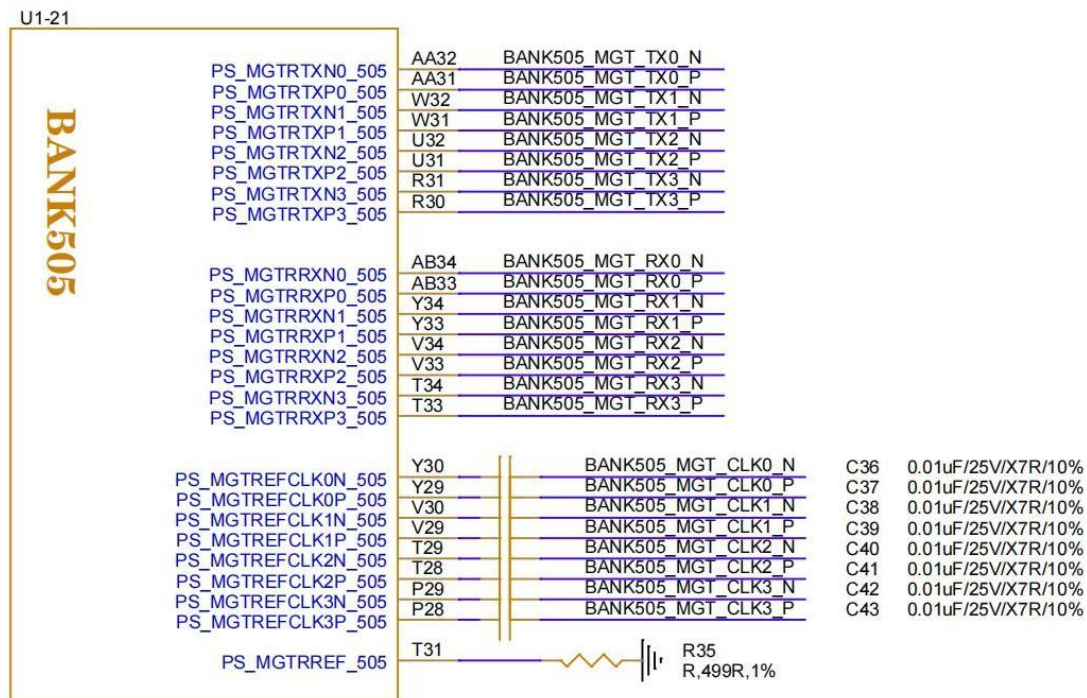


Figure 11 PS End GTR High-Speed Transceiver Mapping Diagram

## 2.8 X PCIe Gen4 Interfaces (requires a PCIe Expansion Card)

RFSOM supports the GTY high-speed transceiver, enabling PCIe x8 Gen4.0 operation with data rates up to 16.0 Gb/s, as well as support for 100G fiber optic interface interconnects. This design facilitates secondary development for users, reduces design risks, and offers high flexibility.

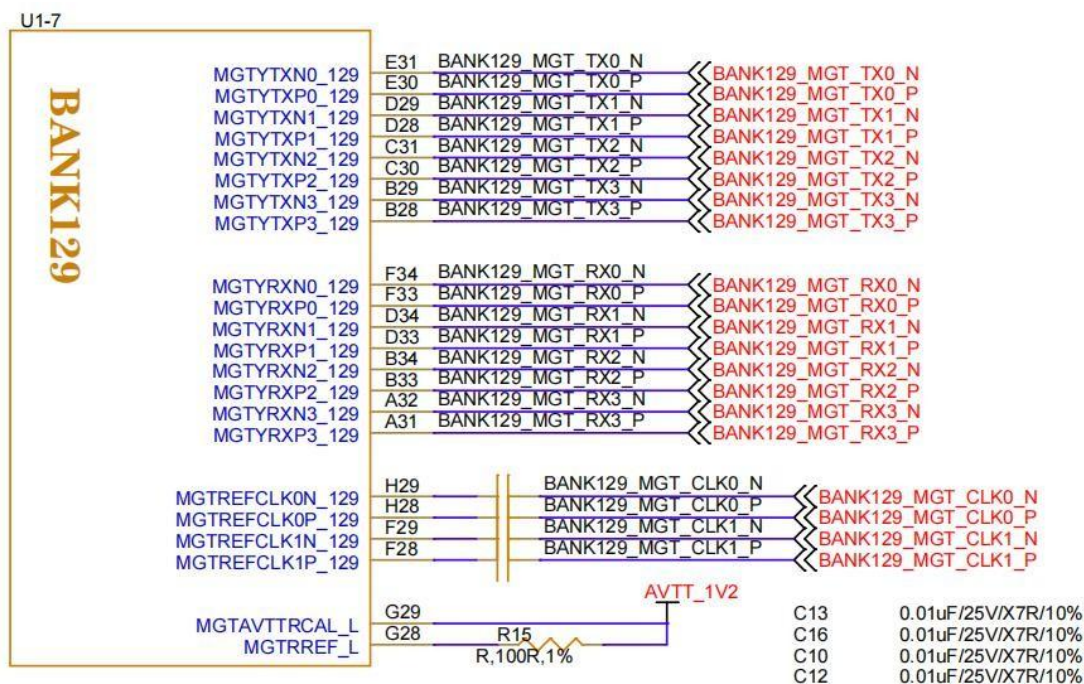


Figure 12 High-Speed Transceiver Mapping Diagram

## 2.9 RF-ADC Interfaces

The FPGA chip used in the RFSOM core module is the Zynq™ UltraScale+™ RFSoc Gen3 series—the only single-chip adaptive radio platform in the industry. This chip integrates a 14-bit RF-ADC with a maximum sampling rate of up to 5 GSPS, and its VCM signal is also routed to a connector, enabling users to easily adjust the common-mode voltage.

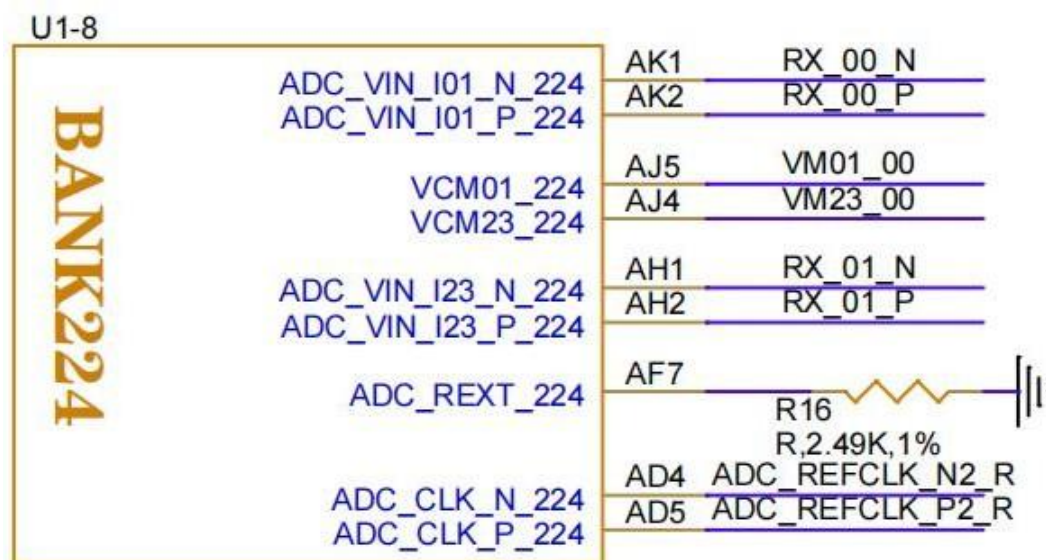


Figure 13: Schematic diagram of the RF-ADC interface

## 2.10 RF-DAC Interfaces

The FPGA chip used in the RFSOM core module is the Zynq™ UltraScale+™ RFSoc Gen3 series—the only single-chip adaptive radio platform in the industry—integrating a 14-bit RF-DAC with a maximum sampling rate of up to 9.85 GSPS.

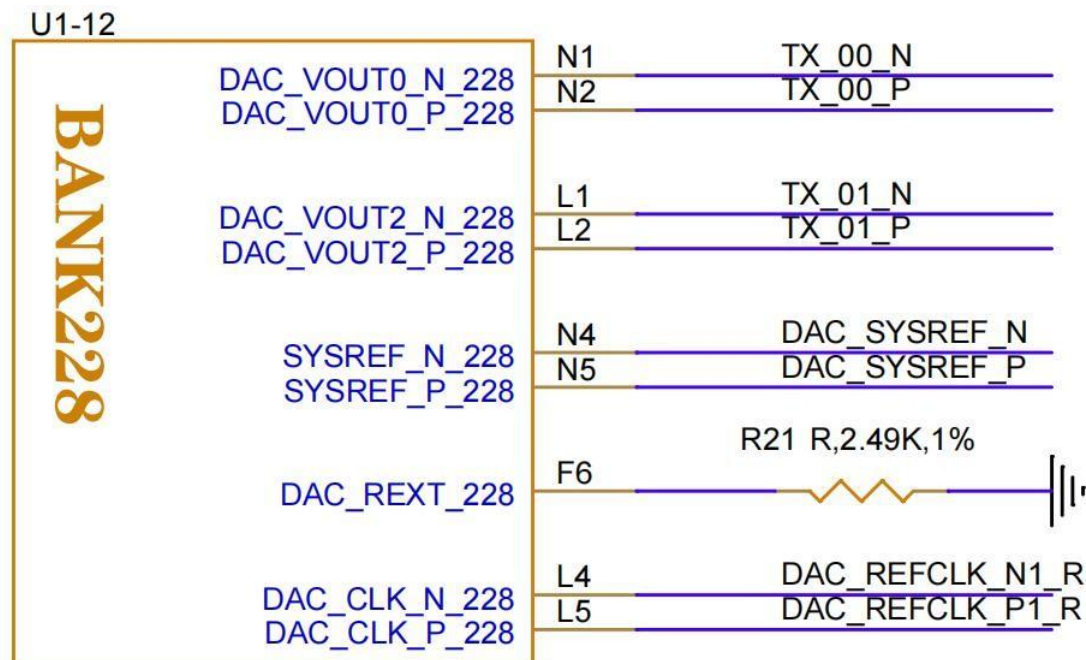


Figure 14: Schematic Diagram of the RF-DAC Interface

## 2.11 Source

The RFSOM core board is powered by a 5 V DC supply, which is delivered from the base board via a connector. The typical power consumption of the RFSOM core board is 60 W. The 5 V system power supply is regulated by a buck regulator to provide various voltages for driving the FPGA and other circuits on the board; the power supply for the board's ADC and DAC is provided by a low-voltage linear LDO, which offers excellent power supply rejection ratio (PSRR).

Below is the level diagram of the IO BANK interface for the core module's expansion:

| BANK    | Voltage level (V)          | Remarks                                                                                                           |
|---------|----------------------------|-------------------------------------------------------------------------------------------------------------------|
| BANK89  | Provided by the base plate | HD_BANK supports 1.2–3.3 V (HD I/O only) at $\pm 5\%$                                                             |
| BANK128 | MGTY                       | PCIe Gen4 signal                                                                                                  |
| BANK129 | MGTY                       | PCIe Gen4 signal                                                                                                  |
| BANK501 | Provided by the base plate | MIO BANK supports 1.8V, 2.5V, and 3.3V at $\pm 5\%$ .                                                             |
| BANK502 | Provided by the base plate | MIO BANK supports 1.8V, 2.5V, and 3.3V at $\pm 5\%$ .                                                             |
| BANK503 | 1.8V Fixed                 | Pin configuration output, mode selection, system reset signal                                                     |
| BANK505 | PS_MGTR                    | No definitions have been specified; all high-speed signal pins and clock signals are terminated at the connector. |

The Power Design Block Diagram of the RFSOM Core Board Is Shown Below:

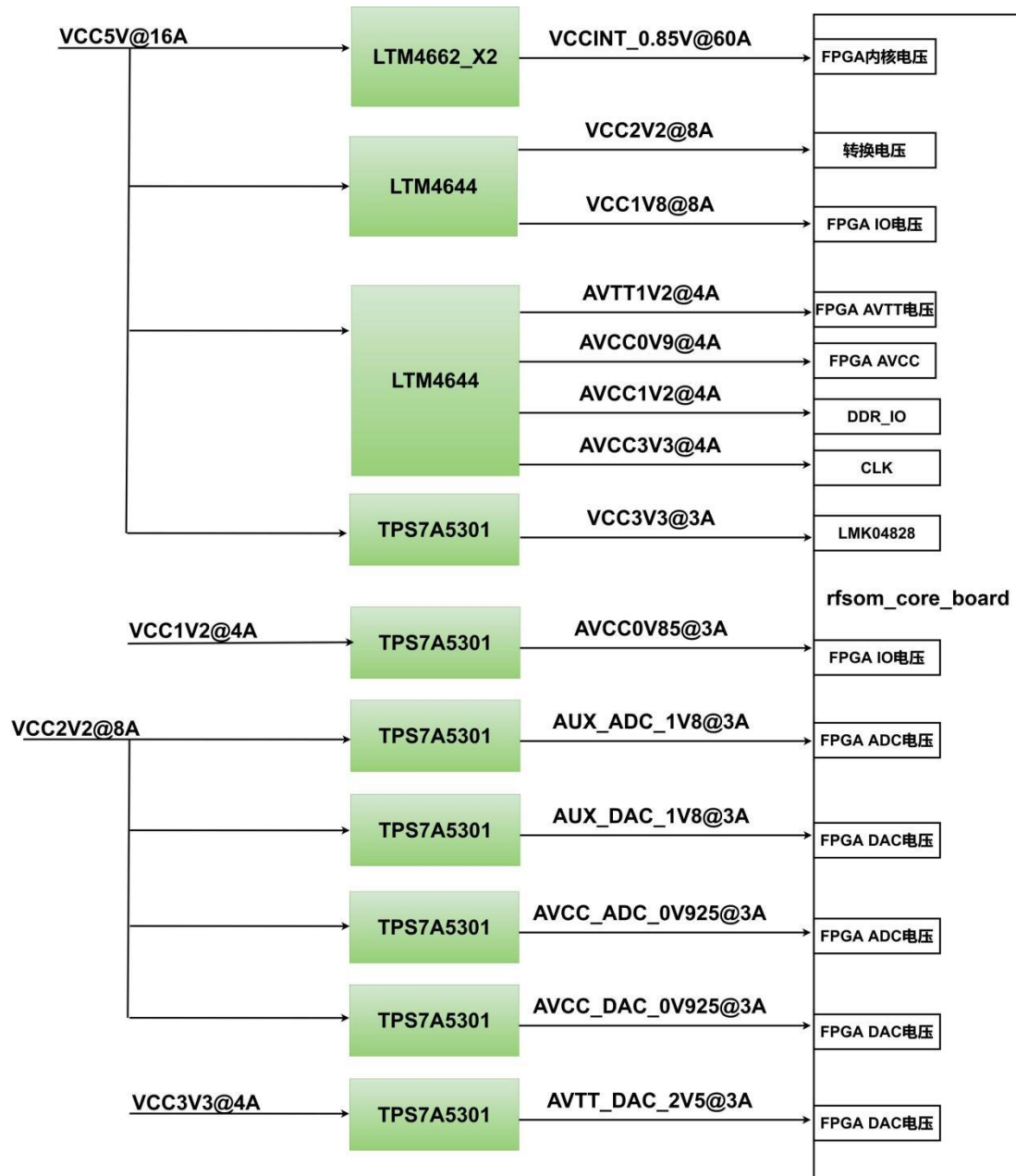


Figure 15 RFSOM Core Board Power Design Block Diagram

## 2.12. Block Diagram

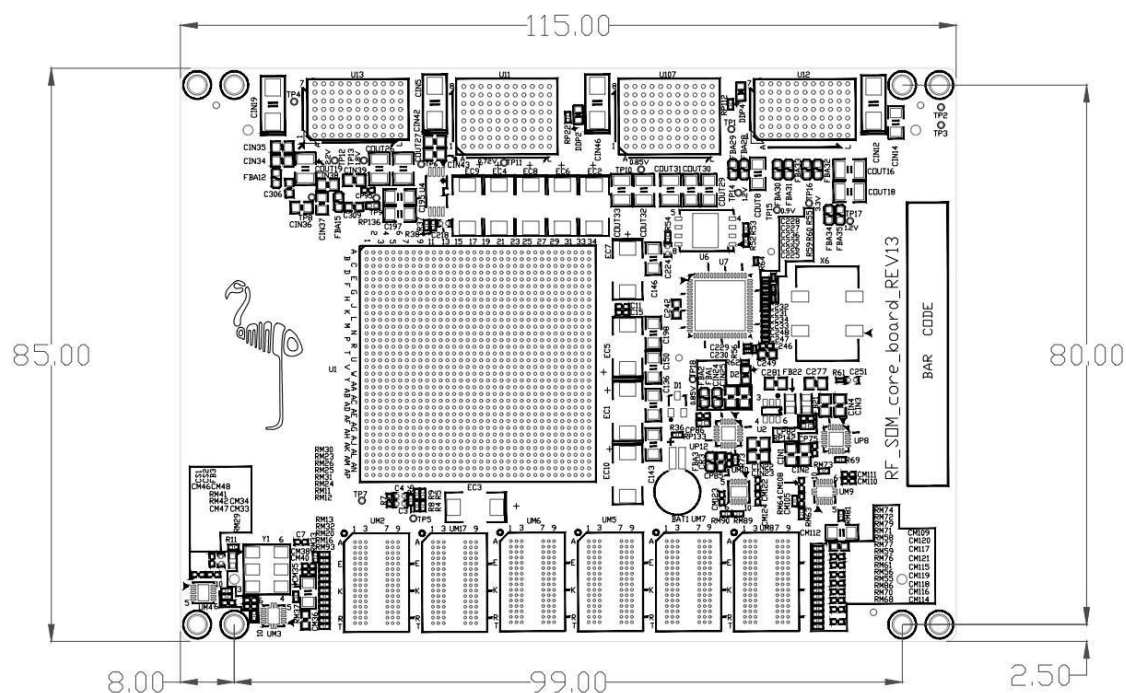


Figure 16: Front View of the RFSOM Core Module

### 2.13 Connector Pin Definition

The core board provides two high-speed expansion ports, which are connected to the base board via two 400-pin board-to-board connectors (J1 and J2); these connectors utilize Samtec's LPAM\_50\_01\_0\_L\_08\_2\_K\_TR connectors.

The signal definitions for the connector are as follows:

Table 5 J1 Connector Signal Definitions

| Reference Number | Signal  | Reference Number | Signal Network | Reference Number | Signal Network | Reference Number | Signal Network |
|------------------|---------|------------------|----------------|------------------|----------------|------------------|----------------|
|                  | Network |                  |                |                  |                |                  |                |
| A1               | GND     | B1               | VCC_5V         | C1               | VCC_5V         | D1               | VCC_5V         |
| A2               | GND     | B2               | VCC_5V         | C2               | VCC_5V         | D2               | VCC_5V         |
| A3               | GND     | B3               | GND            | C3               | GND            | D3               | GND            |
| A4               | GND     | B4               | GND            | C4               | GND            | D4               | GND            |
| A5               | GND     | B5               | GND            | C5               | GND            | D5               | GND            |
| A6               | GND     | B6               | GND            | C6               | GND            | D6               | GND            |
| A7               | GND     | B7               | BANK89_IO_L1P  | C7               | BANK89_IO_L1N  | D7               | GND            |
| A8               | GND     | B8               | GND            | C8               | GND            | D8               | BANK89_IO_L2P  |

|     |     |     |                  |     |                  |     |                  |
|-----|-----|-----|------------------|-----|------------------|-----|------------------|
| A9  | GND | B9  | BANK89_IO_L3P    | C9  | BANK89_IO_L3N    | D9  | GND              |
| A10 | GND | B10 | GND              | C10 | GND              | D10 | BANK89_IO_GC_L5P |
| A11 | GND | B11 | BANK89_IO_GC_L7P | C11 | BANK89_IO_GC_L7N | D11 | GND              |
| A12 | GND | B12 | GND              | C12 | GND              | D12 | BANK89_IO_GC_L6P |
| A13 | GND | B13 | BANK89_IO_L4P    | C13 | BANK89_IO_L4N    | D13 | GND              |
| A14 | GND | B14 | GND              | C14 | GND              | D14 | BANK89_IO_L9P    |
| A15 | GND | B15 | GND              | C15 | GND              | D15 | GND              |
| A16 | GND | B16 | GND              | C16 | GND              | D16 | GND              |
| A17 | GND | B17 | GND              | C17 | GND              | D17 | GND              |
| A18 | GND | B18 | TX_06_P          | C18 | TX_06_N          | D18 | GND              |
| A19 | GND | B19 | GND              | C19 | GND              | D19 | GND              |
| A20 | GND | B20 | GND              | C20 | GND              | D20 | GND              |
| A21 | GND | B21 | GND              | C21 | GND              | D21 | GND              |
| A22 | GND | B22 | TX_04_P          | C22 | TX_04_N          | D22 | GND              |
| A23 | GND | B23 | GND              | C23 | GND              | D23 | GND              |
| A24 | GND | B24 | GND              | C24 | GND              | D24 | GND              |
| A25 | GND | B25 | GND              | C25 | GND              | D25 | GND              |
| A26 | GND | B26 | TX_02_P          | C26 | TX_02_N          | D26 | GND              |
| A27 | GND | B27 | GND              | C27 | GND              | D27 | GND              |
| A28 | GND | B28 | GND              | C28 | GND              | D28 | GND              |
| A29 | GND | B29 | GND              | C29 | GND              | D29 | GND              |
| A30 | GND | B30 | TX_00_P          | C30 | TX_00_N          | D30 | GND              |
| A31 | GND | B31 | GND              | C31 | GND              | D31 | GND              |
| A32 | GND | B32 | GND              | C32 | GND              | D32 | GND              |
| A33 | GND | B33 | GND              | C33 | GND              | D33 | NC               |
| A34 | GND | B34 | RX_06_P          | C34 | RX_06_N          | D34 | GND              |
| A35 | GND | B35 | GND              | C35 | GND              | D35 | GND              |
| A36 | GND | B36 | GND              | C36 | GND              | D36 | GND              |
| A37 | GND | B37 | GND              | C37 | GND              | D37 | NC               |

|     |     |     |         |     |         |     |     |
|-----|-----|-----|---------|-----|---------|-----|-----|
| A38 | GND | B38 | RX_04_P | C38 | RX_04_N | D38 | GND |
| A39 | GND | B39 | GND     | C39 | GND     | D39 | GND |
| A40 | GND | B40 | GND     | C40 | GND     | D40 | GND |
| A41 | GND | B41 | GND     | C41 | GND     | D41 | NC  |
| A42 | GND | B42 | RX_02_P | C42 | RX_02_N | D42 | GND |
| A43 | GND | B43 | GND     | C43 | GND     | D43 | GND |
| A44 | GND | B44 | GND     | C44 | GND     | D44 | GND |
| A45 | GND | B45 | GND     | C45 | GND     | D45 | NC  |
| A46 | GND | B46 | RX_00_P | C46 | RX_00_N | D46 | GND |
| A47 | GND | B47 | GND     | C47 | GND     | D47 | GND |
| A48 | GND | B48 | GND     | C48 | GND     | D48 | GND |
| A49 | GND | B49 | GND     | C49 | GND     | D49 | GND |
| A50 | GND | B50 | GND     | C50 | GND     | D50 | GND |

Table 6 J1 Connector Signal Definitions

| Reference Number | Signal Network   | Reference Number | Signal Network   | Reference Number | Signal Network   | Reference Number | Signal Network |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------|
| E1               | VCC_5V           | F1               | VCC_5V           | G1               | VCC_5V           | H1               | GND            |
| E2               | VCC_5V           | F2               | VCC_5V           | G2               | VCC_5V           | H2               | GND            |
| E3               | GND              | F3               | GND              | G3               | GND              | H3               | GND            |
| E4               | GND              | F4               | GND              | G4               | GND              | H4               | GND            |
| E5               | GND              | F5               | GND              | G5               | GND              | H5               | GND            |
| E6               | GND              | F6               | GND              | G6               | GND              | H6               | GND            |
| E7               | GND              | F7               | BANK89_IO_L12P   | G7               | BANK89_IO_L12N   | H7               | GND            |
| E8               | BANK89_IO_L2N    | F8               | GND              | G8               | GND              | H8               | GND            |
| E9               | GND              | F9               | BANK89_IO_GC_L8P | G9               | BANK89_IO_GC_L8N | H9               | GND            |
| E10              | BANK89_IO_GC_L5N | F10              | GND              | G10              | GND              | H10              | GND            |
| E11              | GND              | F11              | BANK89_IO_L10P   | G11              | BANK89_IO_L10N   | H11              | GND            |
| E12              | BANK89_IO_GC_L6N | F12              | GND              | G12              | GND              | H12              | GND            |

|     |               |     |                |     |                |     |     |
|-----|---------------|-----|----------------|-----|----------------|-----|-----|
| E13 | GND           | F13 | BANK89_IO_L11P | G13 | BANK89_IO_L11N | H13 | GND |
| E14 | BANK89_IO_L9N | F14 | GND            | G14 | GND            | H14 | GND |
| E15 | GND           | F15 | GND            | G15 | GND            | H15 | GND |
| E16 | GND           | F16 | GND            | G16 | GND            | H16 | GND |
| E17 | GND           | F17 | GND            | G17 | GND            | H17 | GND |
| E18 | GND           | F18 | TX_07_P        | G18 | TX_07_N        | H18 | GND |
| E19 | GND           | F19 | GND            | G19 | GND            | H19 | GND |
| E20 | GND           | F20 | GND            | G20 | GND            | H20 | GND |
| E21 | GND           | F21 | GND            | G21 | GND            | H21 | GND |
| E22 | GND           | F22 | TX_05_P        | G22 | TX_05_N        | H22 | GND |
| E23 | GND           | F23 | GND            | G23 | GND            | H23 | GND |
| E24 | GND           | F24 | GND            | G24 | GND            | H24 | GND |
| E25 | GND           | F25 | GND            | G25 | GND            | H25 | GND |
| E26 | GND           | F26 | TX_03_P        | G26 | TX_03_N        | H26 | GND |
| E27 | GND           | F27 | GND            | G27 | GND            | H27 | GND |
| E28 | GND           | F28 | GND            | G28 | GND            | H28 | GND |
| E29 | GND           | F29 | GND            | G29 | GND            | H29 | GND |
| E30 | GND           | F30 | TX_01_P        | G30 | TX_01_N        | H30 | GND |
| E31 | GND           | F31 | GND            | G31 | GND            | H31 | GND |
| E32 | GND           | F32 | GND            | G32 | GND            | H32 | GND |
| E33 | GND           | F33 | GND            | G33 | GND            | H33 | GND |
| E34 | GND           | F34 | RX_07_P        | G34 | RX_07_N        | H34 | GND |
| E35 | NC            | F35 | GND            | G35 | GND            | H35 | GND |
| E36 | GND           | F36 | GND            | G36 | GND            | H36 | GND |
| E37 | GND           | F37 | GND            | G37 | GND            | H37 | GND |
| E38 | GND           | F38 | RX_05_P        | G38 | RX_05_N        | H38 | GND |
| E39 | NC            | F39 | GND            | G39 | GND            | H39 | GND |
| E40 | GND           | F40 | GND            | G40 | GND            | H40 | GND |
| E41 | GND           | F41 | GND            | G41 | GND            | H41 | GND |

|     |     |     |         |     |         |     |     |
|-----|-----|-----|---------|-----|---------|-----|-----|
| E42 | GND | F42 | RX_03_P | G42 | RX_03_N | H42 | GND |
| E43 | NC  | F43 | GND     | G43 | GND     | H43 | GND |
| E44 | GND | F44 | GND     | G44 | GND     | H44 | GND |
| E45 | GND | F45 | GND     | G45 | GND     | H45 | GND |
| E46 | GND | F46 | RX_01_P | G46 | RX_01_N | H46 | GND |
| E47 | NC  | F47 | GND     | G47 | GND     | H47 | GND |
| E48 | GND | F48 | GND     | G48 | GND     | H48 | GND |
| E49 | GND | F49 | GND     | G49 | GND     | H49 | GND |
| E50 | GND | F50 | GND     | G50 | GND     | H50 | GND |

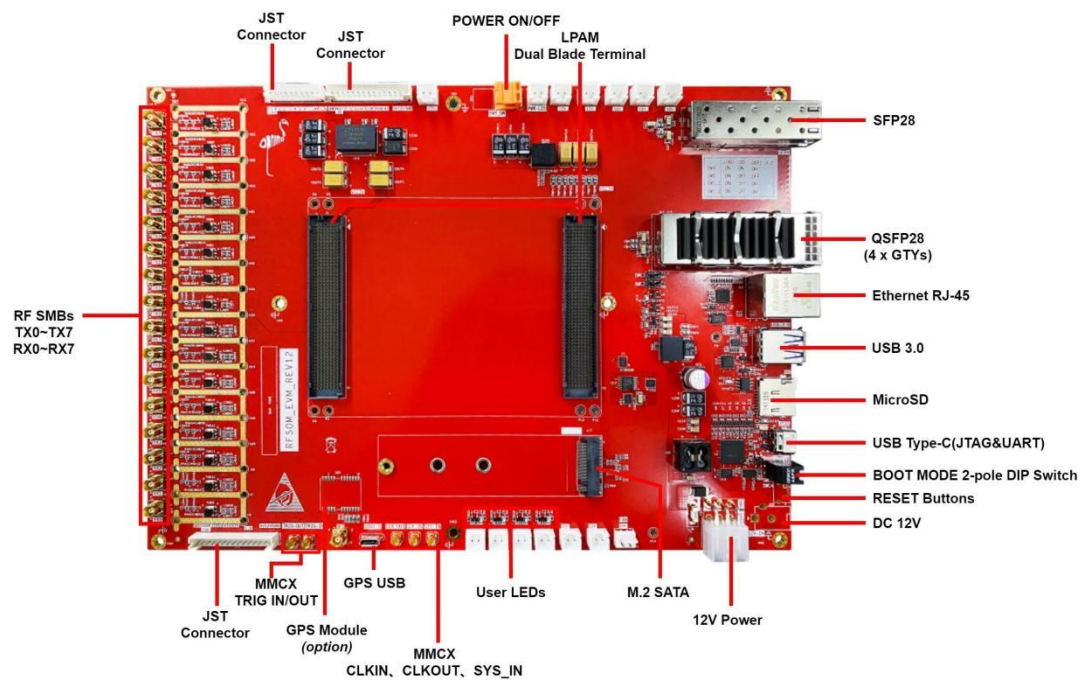
Table 7 J2 Connector Signal Definitions

| Reference<br>Number | Signal Network   | Reference<br>Number | Signal Network   | Reference<br>Number | Signal Network   | Reference<br>Number | Signal<br>Network |
|---------------------|------------------|---------------------|------------------|---------------------|------------------|---------------------|-------------------|
| E1                  | VCCO_501         | F1                  | VCC_5V           | G1                  | VCC_5V           | H1                  | GND               |
| E2                  | VCCO_501         | F2                  | VCC_501          | G2                  | VCC_5V           | H2                  | GND               |
| E3                  | GND              | F3                  | GND              | G3                  | GND              | H3                  | GND               |
| E4                  | GND              | F4                  | CLKIN0_P         | G4                  | CLKIN0_N         | H4                  | GND               |
| E5                  | SYSREF_IN_N      | F5                  | GND              | G5                  | GND              | H5                  | GND               |
| E6                  | GND              | F6                  | GND              | G6                  | GND              | H6                  | GND               |
| E7                  | GND              | F7                  | BANK501_PS_MIO37 | G7                  | BANK501_PS_MIO34 | H7                  | GND               |
| E8                  | BANK501_PS_MIO36 | F8                  | GND              | G8                  | GND              | H8                  | GND               |
| E9                  | GND              | F9                  | BANK501_PS_MIO41 | G9                  | BANK501_PS_MIO38 | H9                  | GND               |
| E10                 | BANK501_PS_MIO39 | F10                 | GND              | G10                 | GND              | H10                 | GND               |
| E11                 | GND              | F11                 | BANK501_PS_MIO43 | G11                 | BANK501_PS_MIO44 | H11                 | GND               |
| E12                 | BANK501_PS_MIO45 | F12                 | GND              | G12                 | GND              | H12                 | GND               |
| E13                 | GND              | F13                 | BANK501_PS_MIO48 | G13                 | BANK501_PS_MIO51 | H13                 | GND               |
| E14                 | BANK501_PS_MIO47 | F14                 | GND              | G14                 | GND              | H14                 | GND               |
| E15                 | GND              | F15                 | BANK501_PS_MIO58 | G15                 | BANK501_PS_MIO60 | H15                 | GND               |
| E16                 | BANK501_PS_MIO59 | F16                 | GND              | G16                 | GND              | H16                 | GND               |

|     |                    |     |                    |     |                    |     |     |
|-----|--------------------|-----|--------------------|-----|--------------------|-----|-----|
| E17 | GND                | F17 | BANK501_PS_MIO63   | G17 | BANK501_PS_MIO62   | H17 | GND |
| E18 | BANK501_PS_MIO55   | F18 | GND                | G18 | GND                | H18 | GND |
| E19 | GND                | F19 | BANK501_PS_MIO64   | G19 | BANK501_PS_MIO65   | H19 | GND |
| E20 | BANK501_PS_MIO71   | F20 | GND                | G20 | GND                | H20 | GND |
| E21 | GND                | F21 | BANK501_PS_MIO75   | G21 | BANK501_PS_MIO70   | H21 | GND |
| E22 | BANK501_PS_MIO74   | F22 | GND                | G22 | GND                | H22 | GND |
| E23 | GND                | F23 | JTAG_TDI           | G23 | PS_ERROR           | H23 | GND |
| E24 | BANK501_PS_MIO77   | F24 | GND                | G24 | GND                | H24 | GND |
| E25 | GND                | F25 | PS_MODE2           | G25 | PS_MODE0           | H25 | GND |
| E26 | PS_MODE1           | F26 | GND                | G26 | GND                | H26 | GND |
| E27 | GND                | F27 | NC                 | G27 | NC                 | H27 | GND |
| E28 | JTAG_TCK           | F28 | GND                | G28 | GND                | H28 | GND |
| E29 | GND                | F29 | BANK129_MGT_RX1_P  | G29 | BANK129_MGT_RX1_N  | H29 | GND |
| E30 | BANK129_MGT_RX2_N  | F30 | GND                | G30 | GND                | H30 | GND |
| E31 | GND                | F31 | BANK129_MGT_TX2_P  | G31 | BANK129_MGT_TX2_N  | H31 | GND |
| E32 | BANK129_MGT_TX3_N  | F32 | GND                | G32 | GND                | H32 | GND |
| E33 | GND                | F33 | BANK505_MGT_CLK0_P | G33 | BANK505_MGT_CLK0_N | H33 | GND |
| E34 | BANK129_MGT_TX0_N  | F34 | GND                | G34 | GND                | H34 | GND |
| E35 | GND                | F35 | BANK505_MGT_CLK3_P | G35 | BANK505_MGT_CLK3_N | H35 | GND |
| E36 | BANK505_MGT_CLK2_N | F36 | GND                | G36 | GND                | H36 | GND |
| E37 | GND                | F37 | BANK128_MGT_RX1_P  | G37 | BANK128_MGT_RX1_N  | H37 | GND |
| E38 | BANK128_MGT_RX2_N  | F38 | GND                | G38 | GND                | H38 | GND |
| E39 | GND                | F39 | BANK128_MGT_TX2_P  | G39 | BANK128_MGT_TX2_N  | H39 | GND |
| E40 | BANK128_MGT_CLK1_N | F40 | GND                | G40 | GND                | H40 | GND |
| E41 | GND                | F41 | BANK128_MGT_TX0_P  | G41 | BANK128_MGT_TX0_N  | H41 | GND |
| E42 | BANK128_MGT_TX1_N  | F42 | GND                | G42 | GND                | H42 | GND |
| E43 | GND                | F43 | BANK505_MGT_TX2_P  | G43 | BANK505_MGT_TX2_N  | H43 | GND |
| E44 | BANK505_MGT_TX1_N  | F44 | GND                | G44 | GND                | H44 | GND |
| E45 | GND                | F45 | BANK505_MGT_RX2_P  | G45 | BANK505_MGT_RX2_N  | H45 | GND |

|     |                   |     |                    |     |                    |     |     |
|-----|-------------------|-----|--------------------|-----|--------------------|-----|-----|
| E46 | BANK505_MGT_RX3_N | F46 | GND                | G46 | GND                | H46 | GND |
| E47 | GND               | F47 | BANK129_MGT_CLK1_N | G47 | BANK129_MGT_CLK1_P | H47 | GND |
| E48 | BANK505_MGT_RX0_N | F48 | GND                | G48 | GND                | H48 | GND |
| E49 | GND               | F49 | GND                | G49 | GND                | H49 | GND |
| E50 | GND               | F50 | GND                | G50 | GND                | H50 | GND |

### 3 Support Plate



### 3.1 Brief Introduction

From the previous feature overview, we have gained insight into some of the capabilities of the carrier plate.

- 1 x M.2 port
- 1 x USB 3.0 port
- 1 x Gigabit Ethernet interface

- Type-C interface with 1 JTAG & UART lane
- 1 x Micro SD card slot
- 1 x SFP optical port
- 1 x QSFP28 optical port
- Two groups use PL extended IOx8, and one group uses PS extended IO.
- 4 user LED lights

### 3.2 M.2 Interface

The RFEVM development board features a standard PCIe x2 M.2 interface for connecting M.2 SSDs. The M.2 interface utilizes an M-key slot, supporting only PCIe and not SATA; therefore, when selecting an SSD, users must choose a PCIe-type SSD.

The PCIe signal is directly connected to the BANK505 PS MGT transceiver of the ZU47DR; the two TX and RX signals are both connected to LANE0 and LANE1 of the MGT in differential mode. The PCIe clock is provided by a 100 MHz differential clock. A schematic diagram of the M.2 circuit design is shown below:

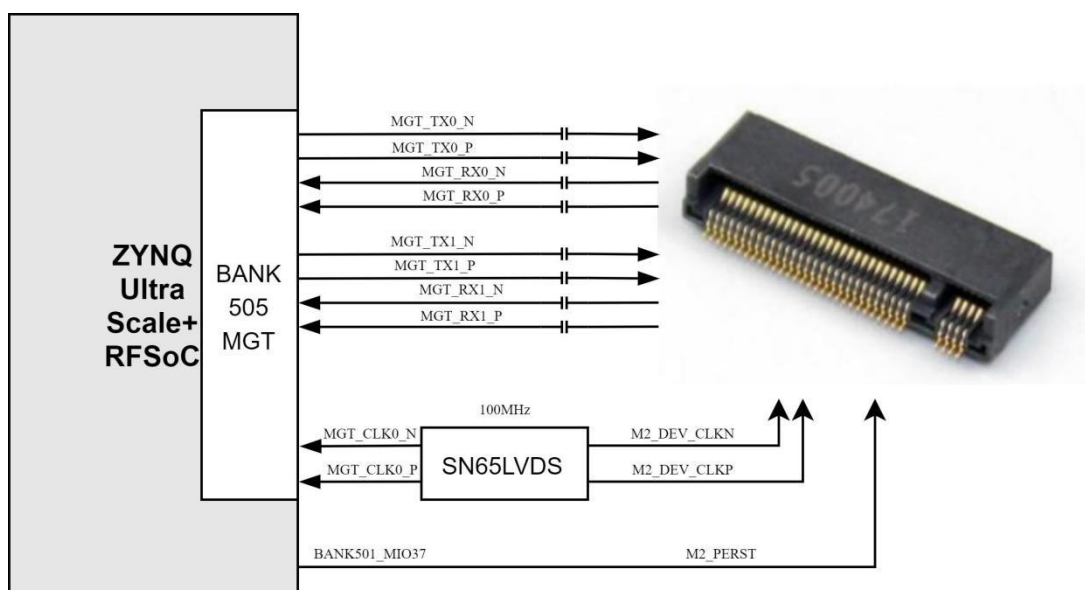


Figure 17 M.2 Schematic Diagram of Interface Design

Table 8: M.2 Interface ZYNQ Pin Assignment

| Signal Name | ZYNQ Pin Numbers | M.2 Connector J17 |       |
|-------------|------------------|-------------------|-------|
|             |                  | Pin Number        | Name  |
| MGT_TX0_N   | AA32             | 47                | PETn0 |

|            |      |    |       |
|------------|------|----|-------|
| MGT_TX0_P  | AA31 | 49 | PETp0 |
| MGT_TX1_N  | W32  | 35 | PETn1 |
| MGT_TX1_P  | W31  | 37 | PETp1 |
| MGT_RX0_N  | AB34 | 41 | PERn0 |
| MGT_RX0_P  | AB33 | 43 | PERp0 |
| MGT_RX1_N  | Y34  | 29 | PERn1 |
| MGT_RX1_P  | Y33  | 31 | PERp1 |
| MGT_CLK0_N | Y30  |    |       |
| MGT_CLK0_P | Y29  |    |       |

### 3.3 USB 3.0 Ports

The RFEVM board features one USB 3.0 port, supporting both HOST and SLAVE operating modes, with a data transfer rate of up to 5.0 Gb/s. The USB 3.0 port connects directly to an external Type-A interface, while the USB 2.0 port connects to the external USB3320C chip via an ULPI interface, enabling high-speed data communication between USB 3.0 and USB 2.0. The connection schematic for USB 3.0 is shown below:

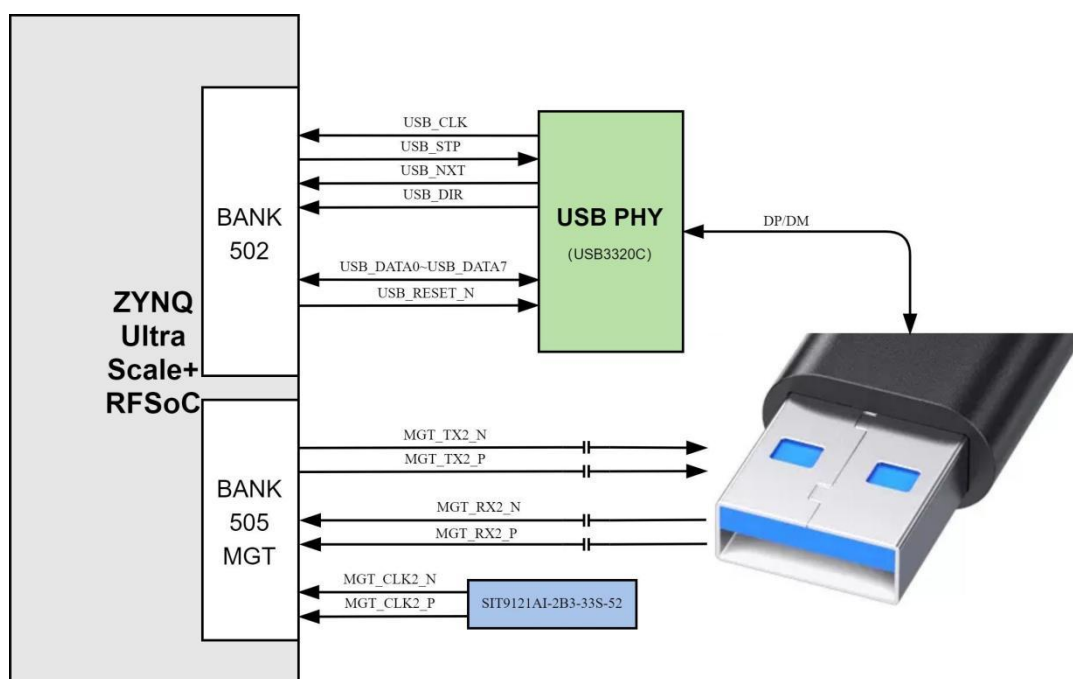


Figure 18: Schematic Diagram of the USB 3.0 Interface

Table 9: USB Interface Pin Assignment

| Signal Name | Pin Name          | ZYNQ Pin Numbers | Remarks                                        |
|-------------|-------------------|------------------|------------------------------------------------|
| USB_TX_N    | BANK505_MGT_TX2_N | U32              | USB 3.0 data transmission failure              |
| USB_TX_P    | BANK505_MGT_TX2_P | U31              | USB 3.0 data transmission is working correctly |
| USB_RX_N    | BANK505_MGT_RX2_N | V34              | USB 3.0 data transfer                          |
| USB_RX_P    | BANK505_MGT_RX2_P | V33              | USB 3.0 data transfer enabled                  |
| USB_DATA0   | BANK502_PS_MIO56  | G23              | USB 2.0 Data Bit 0                             |
| USB_DATA1   | BANK502_PS_MIO57  | F23              | USB 2.0 Data Bit 1                             |
| USB_DATA2   | BANK502_PS_MIO54  | H23              | USB 2.0 Data Bit 2                             |
| USB_DATA3   | BANK502_PS_MIO59  | D23              | USB 2.0 Data Bit 3                             |
| USB_DATA4   | BANK502_PS_MIO60  | A23              | USB 2.0 Data Bit 4                             |
| USB_DATA5   | BANK502_PS_MIO61  | E22              | USB 2.0 Data Bit 5                             |
| USB_DATA6   | BANK502_PS_MIO62  | B23              | USB 2.0 Data Bit 6                             |
| USB_DATA7   | BANK502_PS_MIO63  | C23              | USB 2.0 Data Bit 7                             |
| USB_STP     | BANK502_PS_MIO58  | B22              | USB 2.0 stop signal                            |
| USB_DIR     | BANK502_PS_MIO53  | F22              | USB 2.0 data direction signal                  |
| USB_CLK     | BANK502_PS_MIO52  | G22              | USB 2.0 clock signal                           |
| USB_NXT     | BANK502_PS_MIO55  | D22              | Next data signal on USB 2.0                    |
| USB_RESET_N | BANK501_PS_MIO36  | C18              | USB 2.0 reset signal                           |

### 3.4 Gigabit Ethernet Interface

The RFEVM board features one Gigabit Ethernet interface connected to the PS side. The Ethernet chipset employs Atheros' fourth-generation AR8035 chip to provide network communication services. The Ethernet PHY chip on the PS side is connected to the MIO of BANK502 on the PS side of the ZYNQ system. The AR8035 chip supports network transmission rates of 10/100/1000 Mbps and communicates with the MAC layer of the ZYNQ system via an RGMII interface. The connection schematic of the Gigabit Ethernet PHY chip is shown in the figure below:

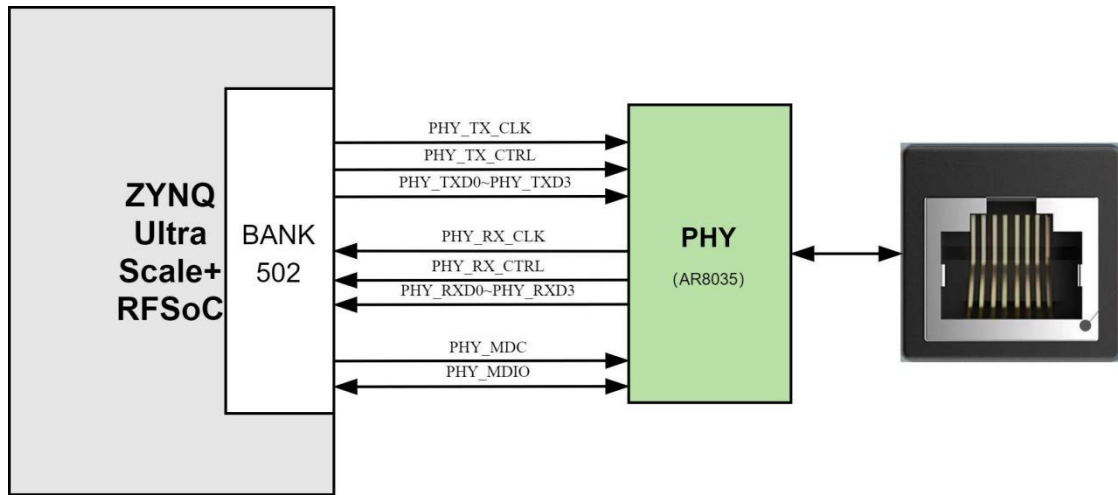


Figure 19 Schematic Diagram of Ethernet Connection

Table 10: AR8035 PHY connected To XCZU47DR RFSoc

| Signal Name | Pin Name         | Pin Number | AR8035 PHY U12 |          |
|-------------|------------------|------------|----------------|----------|
|             |                  |            | Pin Number     | Pin Name |
| PHY_TX_CLK  | BANK502_PS_MIO64 | D24        | 33             | GTX_CLK  |
| PHY_TXD0    | BANK502_PS_MIO65 | C24        | 34             | TXD0     |
| PHY_TXD1    | BANK502_PS_MIO66 | F24        | 35             | TXD1     |
| PHY_TXD2    | BANK502_PS_MIO67 | F25        | 36             | TXD2     |
| PHY_TXD3    | BANK502_PS_MIO68 | E25        | 37             | TXD3     |
| PHY_TX_CTRL | BANK502_PS_MIO69 | E24        | 32             | TX_EN    |
| PHY_RX_CLK  | BANK502_PS_MIO70 | B25        | 31             | RX_CLK   |
| PHY_RXD0    | BANK502_PS_MIO71 | A24        | 29             | RXD0     |
| PHY_RXD1    | BANK502_PS_MIO72 | C25        | 28             | RXD1     |
| PHY_RXD2    | BANK502_PS_MIO73 | A25        | 26             | RXD2     |
| PHY_RXD3    | BANK502_PS_MIO74 | C26        | 25             | RXD3     |
| PHY_RX_CTRL | BANK502_PS_MIO75 | B26        | 30             | RX_DV    |
| PHY_MDC     | BANK502_PS_MIO76 | E26        | 40             | MDC      |
| PHY_MDIO    | BANK502_PS_MIO77 | D26        | 39             | MDIO     |

|          |                  |     |   |      |
|----------|------------------|-----|---|------|
| PS_POR_B | BANK501_PS_MIO44 | C20 | 1 | RSTn |
|----------|------------------|-----|---|------|

### 3.5 Micro SD Card Slots

The RFEVM carrier board features a Micro SD card interface, enabling users to access SD card storage for storing the BOOT program, the Linux operating system kernel, the file system, and other user data files.

The SD card I/O signal is connected to the MIO signal of PS BANK501; the connection schematic between the PS and the SD card connector is shown below:

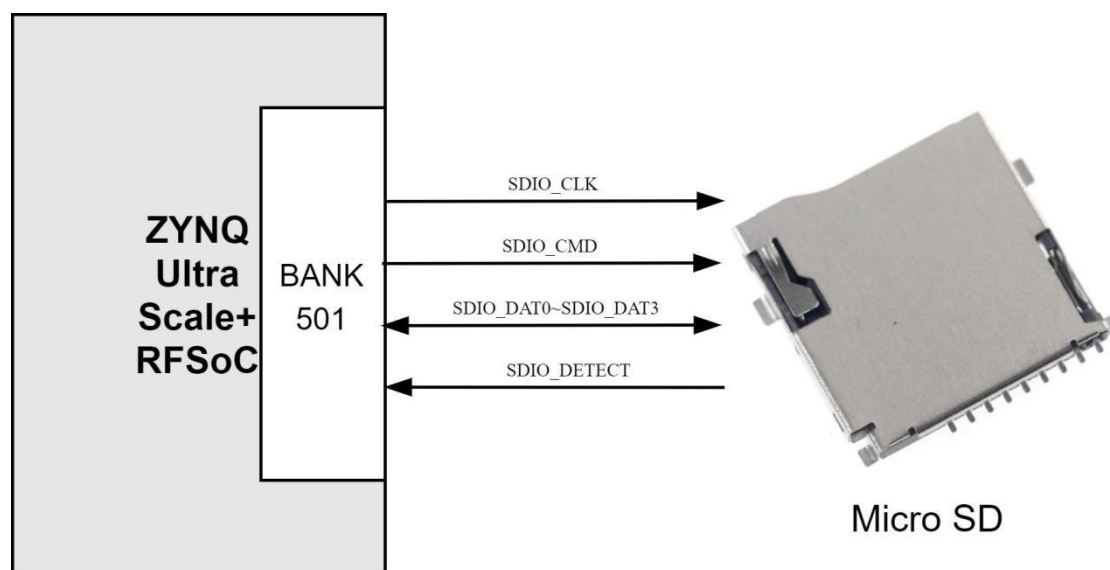


Figure 20 SD Card Connection Schematic Diagram

Table 11 SD Card Pin Assignment

| Signal Name | Pin Name         | Pin Number | Remarks                  |
|-------------|------------------|------------|--------------------------|
| SDIO_CLK    | BANK501_PS_MIO51 | B21        | SDclock signal           |
| SDIO_CMD    | BANK501_PS_MIO50 | A22        | SDcommand signal         |
| SDIO_DAT0   | BANK501_PS_MIO46 | A20        | SD Data Bit 0            |
| SDIO_DAT1   | BANK501_PS_MIO47 | D21        | SD Data Bit 1            |
| SDIO_DAT2   | BANK501_PS_MIO48 | C21        | SD Data Bit 2            |
| SDIO_DAT3   | BANK501_PS_MIO49 | E21        | SD Data Bit 3            |
| SDIO_DETECT | BANK501_PS_MIO45 | B20        | SD card detection signal |

### 3.6 Optical Fiber Interface

The RFEVM board features two fiber optic interfaces, one SFP interface, and one QSFP28 interface. The two fiber optic interfaces are connected to the GTY transceivers on BANK128 and BANK129 of the ZYNQ device, respectively. The two reference clocks on BANK128 are provided by the LMK04828 chip on the RFSOM core board and the differential crystal oscillator on the board, both operating at 156.25 MHz.

The connection schematic diagram of the QSFP28 interface is shown in the figure below:

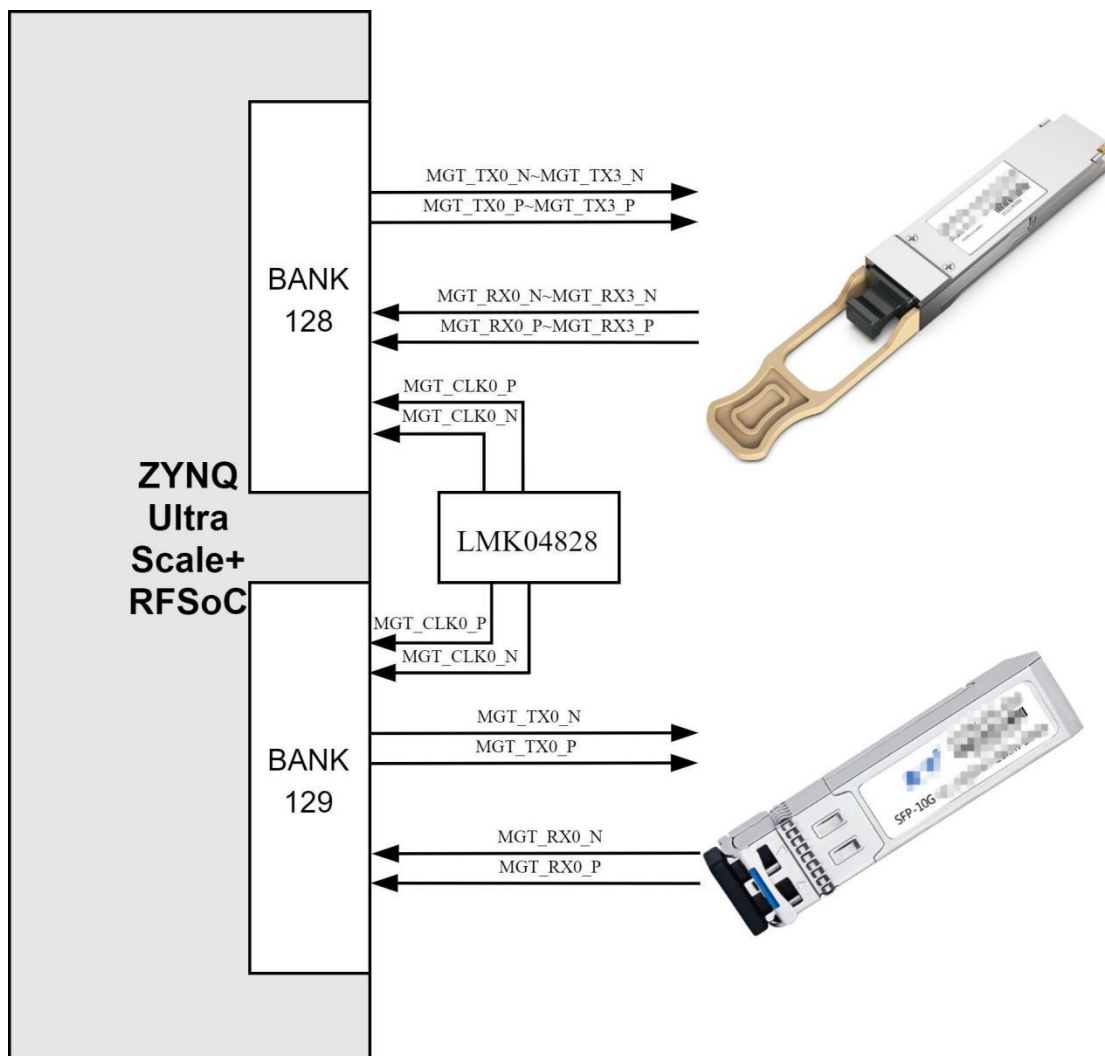


Figure 21 Schematic Diagram of the Optical Fiber Design

Table 12 QSFP Interface Pin Assignment

| Signal Name | ZYNQ Pin Names | ZYNQ Pin Numbers | Remarks |
|-------------|----------------|------------------|---------|
| QSFP_RX0_N  | MGTYRXN0_128   | P34              |         |
| QSFP_RX0_P  | MGTYRXP0_128   | P33              |         |

|            |              |     |  |
|------------|--------------|-----|--|
| QSFP_RX1_N | MGTYRXN1_128 | M34 |  |
| QSFP_RX1_P | MGTYRXP1_128 | M33 |  |
| QSFP_RX2_N | MGTYRXN2_128 | K34 |  |
| QSFP_RX2_P | MGTYRXP2_128 | K33 |  |
| QSFP_RX3_N | MGTYRXN3_128 | H34 |  |
| QSFP_RX3_P | MGTYRXP3_128 | H33 |  |
| QSFP_TX0_N | MGTYTXN0_128 | N31 |  |
| QSFP_TX0_P | MGTYTXP0_128 | N30 |  |
| QSFP_TX1_N | MGTYTXN1_128 | L31 |  |
| QSFP_TX1_P | MGTYTXP1_128 | L30 |  |
| QSFP_TX2_N | MGTYTXN2_128 | J31 |  |
| QSFP_TX2_P | MGTYTXP2_128 | J30 |  |
| QSFP_TX3_N | MGTYTXN3_128 | G31 |  |
| QSFP_TX3_P | MGTYTXP3_128 | G30 |  |

Table 13 BANK128 Reference Clock Allocation

| ZYNQ Pin Names  | ZYNQ Pin Numbers | Remarks                                                                     |
|-----------------|------------------|-----------------------------------------------------------------------------|
| MGTREFCLK0N_128 | M29              | The SDCLKOUT3 output of LMK04828 has a default configuration of 156.25 MHz. |
| MGTREFCLK0P_128 | M28              | The SDCLKOUT3 output of LMK04828 has a default configuration of 156.25 MHz. |
| MGTREFCLK1N_128 | K29              | Carrier board: 156.25 MHz differential output                               |
| MGTREFCLK1P_128 | K28              | Carrier board: 156.25 MHz differential output                               |
| MGTREFCLK0N_129 | H29              | The SDCLKOUT1 output of LMK04828 has a default configuration of 156.25 MHz. |
| MGTREFCLK0P_129 | H28              | The SDCLKOUT1 output of LMK04828 has a default configuration of 156.25 MHz. |

Table 14 SFP Interface Pin Assignment

| Signal Name | ZYNQ Pin Names | ZYNQ Pin Numbers | Remarks |
|-------------|----------------|------------------|---------|
| SFP_RX0_N   | MGTYRXN0_129   | F34              |         |
| SFP_RX0_P   | MGTYRXP0_129   | F33              |         |
| SFP_TX0_N   | MGTYTXN0_129   | E31              |         |
| SFP_TX0_P   | MGTYTXP0_129   | E30              |         |

Low-speed control I/O processing:

Table 15: Low-Speed Fiber Optic I/O Signal Processing Methods

| QSFP Low-speed IO Signal Name | Remarks      | SFP Low-speed IO Signal Name | Remarks      |
|-------------------------------|--------------|------------------------------|--------------|
| SCL                           | Pull up 3.3V | TX_FULT                      | Pull up 3.3V |
| SDA                           | Pull up 3.3V | TX_DISABLE                   | Landing      |
| ModSelL                       | Pull up 3.3V | RATE_SELECT0                 | Pull up 3.3V |
| ResetL                        | Pull up 3.3V | RATE_SELECT1                 | Pull up 3.3V |
| ModPrsL                       | Pull up 3.3V | LOS                          | Pull up 3.3V |
| intL                          | Pull up 3.3V |                              |              |
| LPMODE                        | Landing      |                              |              |

### 3.7 JTAG & UART Interfaces

The RFEVM board features a JTAG & UART interface, which is used to download and debug FPGA programs or to flash programs into FLASH memory. In this implementation, we employ the FT 2232H chip from FTDI—a USB 2.0 high-speed-to-UART/FIFO device chip—equipped with two multi-protocol synchronous serial engines that support JTAG functionality. This chip also offers the capability to configure connections via a variety of industrial-standard serial or parallel interfaces.

The connection schematic for JTAG and UART is shown in the figure below:

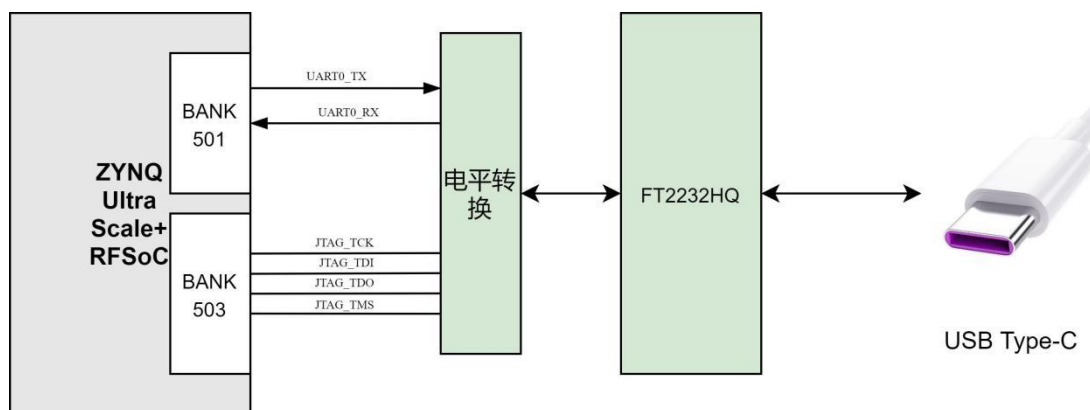


Figure 22: Schematic Diagram of JTAG &amp; UART Connector Connection

| Signal Name | Pin Name         | Pin Number | Remarks            |
|-------------|------------------|------------|--------------------|
| UART0_TX    | BANK501_PS_MIO43 | A19        | PSUart Data Output |
| UART0_RX    | BANK501_PS_MIO42 | E20        | PSUart Data Input  |

### 3.8 GPS Modules (optional)

The RFEVM carrier board can optionally incorporate the GPS module NEO-M8N, a high-performance GNSS receiver module featuring exceptional positioning accuracy and sensitivity. This module utilizes the latest u-blox M8 chipset, supporting multiple satellite systems—including GPS, GLONASS, BeiDou, and Galileo—enabling global positioning data acquisition. The GPS connection schematic is illustrated in the figure below:

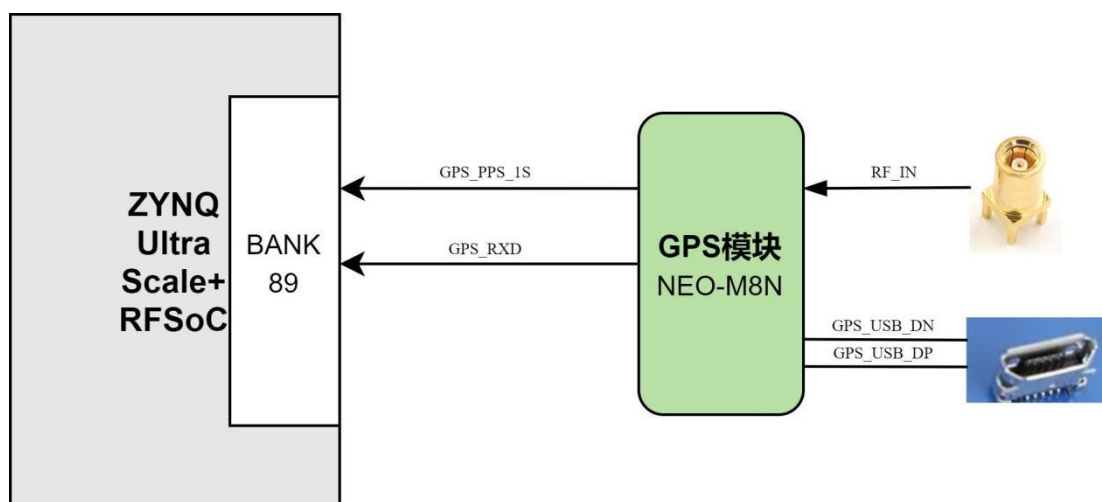


Figure 23: GPS Module Connection Schematic

Table 16: GPS Module Pin Assignment

| Signal Name | Pin Name        | Pin Number | Remarks   |
|-------------|-----------------|------------|-----------|
| GPS_PPS_1S  | IO_L10P_AD2P_89 | K11        | TIMEPLUSE |
| GPS_TXD     | IO_L9P_AD3P_89  | H10        | TXD_MISO  |

### 3.9. Extended I/O and LED Indicator Lights

The RFEVM carrier board extends two sets of PL-end I/Os (x8) and one set of PS-end I/Os (x10).

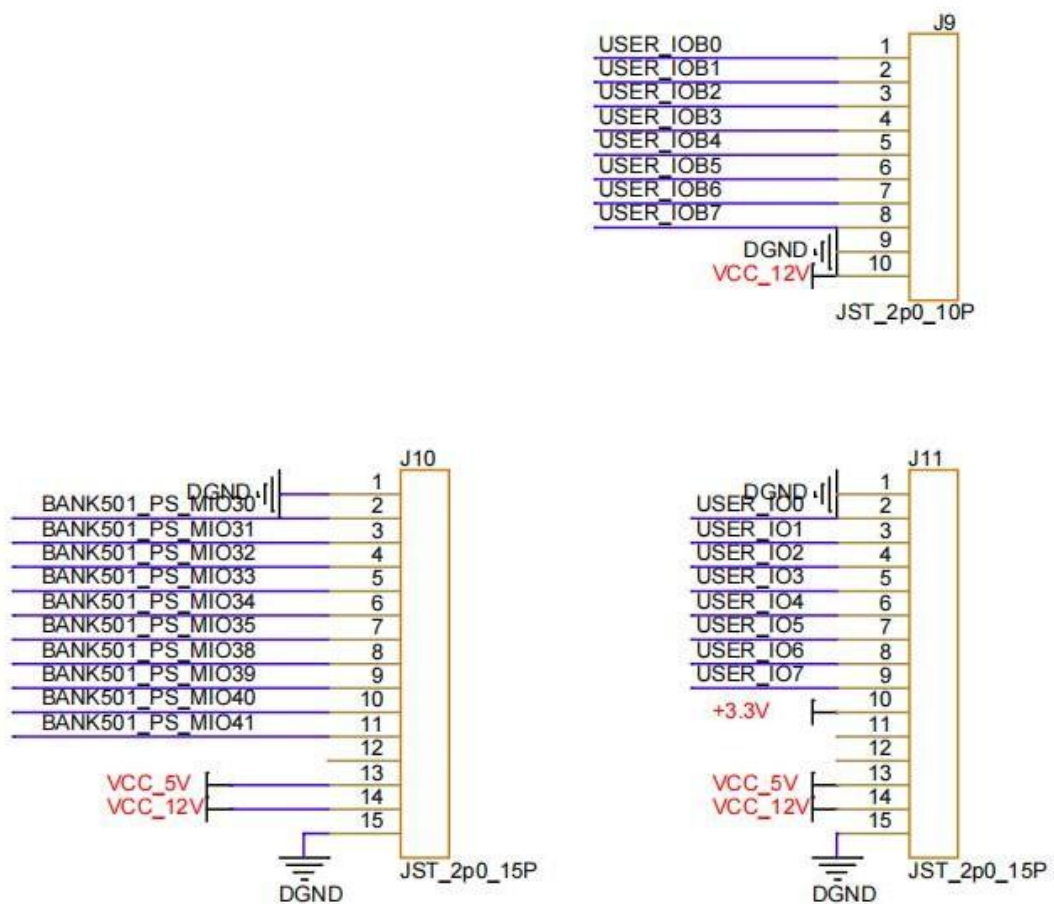


Figure 24 Schematic Diagram of the Extended IO Circuit Connection

Table 17 J11 Extended IO Pin Assignment

| Signal Name | Pin Name            | Pin Number | Remarks |
|-------------|---------------------|------------|---------|
| USER_IO0    | IO_L6N_HDGC_AD6N_89 | E9         |         |
| USER_IO1    | IO_L5P_HDGC_AD7P_89 | E11        |         |

|          |                     |     |  |
|----------|---------------------|-----|--|
| USER_IO2 | IO_L5N_HDGC_AD7N_89 | D11 |  |
| USER_IO3 | IO_L4P_AD8P_89      | D9  |  |
| USER_IO4 | IO_L4N_AD8N_89      | C9  |  |
| USER_IO5 | IO_L3P_AD9P_89      | A10 |  |
| USER_IO6 | IO_L3N_AD9N_89      | A9  |  |
| USER_IO7 | IO_L2P_AD10P_89     | C10 |  |

Table 18 J9 Extended IO Pin Assignment

| Signal Name | Pin Name            | Pin Number | Remarks |
|-------------|---------------------|------------|---------|
| USER_IOB0   | IO_L10N_AD2N_89     | K10        |         |
| USER_IOB1   | IO_L11P_AD1P_89     | J11        |         |
| USER_IOB2   | IO_L11N_AD1N_89     | H11        |         |
| USER_IOB3   | IO_L8P_HDGC_AD4P_89 | G11        |         |
| USER_IOB4   | IO_L8N_HDGC_AD4N_89 | G10        |         |
| USER_IOB5   | IO_L7P_HDGC_AD5P_89 | F10        |         |
| USER_IOB6   | IO_L7N_HDGC_AD5N_89 | F9         |         |
| USER_IOB7   | IO_L6P_HDGC_AD6P_89 | E10        |         |

Table 19 J10 Extended IO Pin Assignment

| Signal Name      | Pin Name | Pin Number | Remarks |
|------------------|----------|------------|---------|
| BANK501_PS_MIO30 | PS_MIO30 | H20        |         |
| BANK501_PS_MIO31 | PS_MIO31 | G20        |         |
| BANK501_PS_MIO32 | PS_MIO32 | F19        |         |
| BANK501_PS_MIO33 | PS_MIO33 | G21        |         |
| BANK501_PS_MIO34 | PS_MIO34 | D18        |         |
| BANK501_PS_MIO35 | PS_MIO35 | F20        |         |
| BANK501_PS_MIO38 | PS_MIO38 | B18        |         |
| BANK501_PS_MIO39 | PS_MIO39 | D19        |         |

|                  |          |     |  |
|------------------|----------|-----|--|
| BANK501_PS_MIO40 | PS_MIO40 | A18 |  |
| BANK501_PS_MIO41 | PS_MIO41 | C19 |  |

The RFEVM carrier board supports the expansion of up to four user-defined LED indicators, with four additional I/O pins connected to the 2-pin TJC3 header.

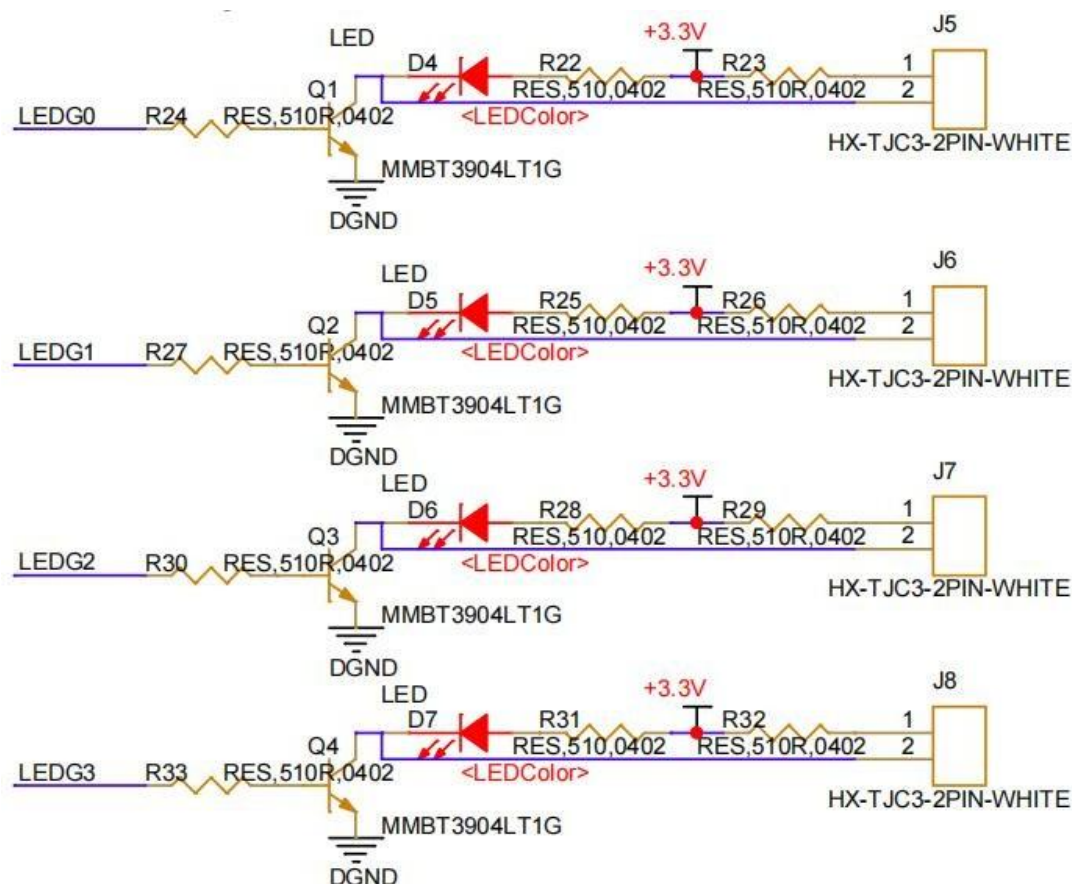


Figure 25: Schematic Diagram of the LED Lamp I/O Expansion Circuit

Table 20: LED Lamp Extended IO Pin Allocation

| Signal Name | Pin Name        | Pin Number | Remarks |
|-------------|-----------------|------------|---------|
| LEDG0       | IO_L9N_AD3N_89  | H9         |         |
| LEDG1       | IO_L1N_AD11N_89 | B11        |         |
| LEDG2       | IO_L2N_AD10N_89 | B10        |         |
| LEDG3       | IO_L1P_AD11P_89 | C11        |         |

### 3.10. DIP Switch Configuration

The RFEVM development board features a 2-bit DIP switch SWC1 and two jumper caps for configuring the boot mode of the ZYNQ system. The RFEVM development platform supports three boot modes: JTAG debug mode, QSPI FLASH mode, and SD card boot mode. Upon power-up, the RFSoc chip detects the voltage levels of (PS\_MODE0~3) to determine which boot mode to activate. Users can select different boot modes via the DIP switch SWC1.

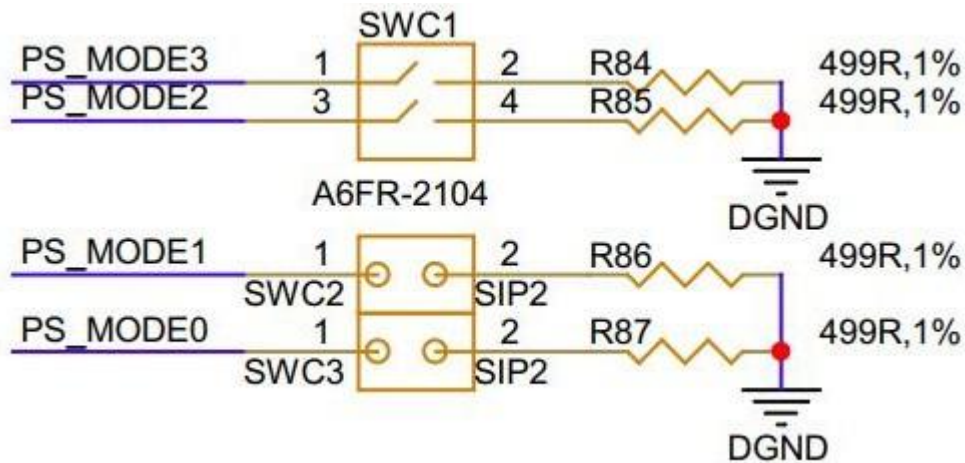
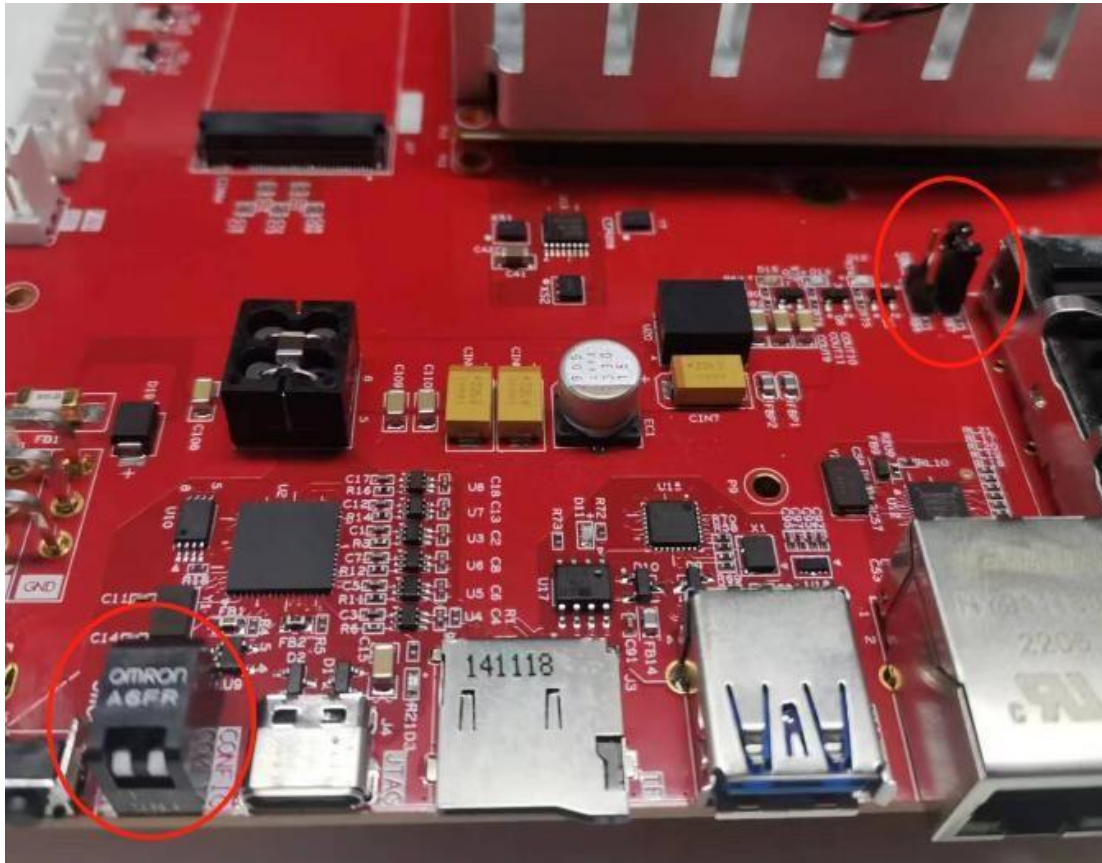


Figure 26: PS\_MODE Circuit Schematic

By default, SWC3 is set to short-circuit via the jumper cap (i.e., PS\_MODE0=0), while SWC2 is set to pull-up by default (i.e., PS\_MODE1=1).



The startup mode configuration for SWC1 is shown in the table below.

Table 21 SWC1 Startup Mode Configuration

| DIP Switch SWC1 Position ( 1 , 2 ) | MODE[3:0] | Startup Mode |
|------------------------------------|-----------|--------------|
| <del>ON</del> , <del>ON</del>      | 0000      | JTAG         |
| ON, ON                             | 0010      | QSPI         |
| <del>ON</del> , <del>OFF</del>     | 0110      | EMMC         |
| OFF, OFF                           | 1110      | SD           |

Note: In SD card boot mode, the JTAG functionality remains fully operational.

### 3.11 Source

The RFEVM development board has a DC12V power input voltage, and the board utilizes multiple power supply chips to generate +5V, +1.8V, and +3.3V power supplies.

The power supply design block diagram is shown in the figure below:

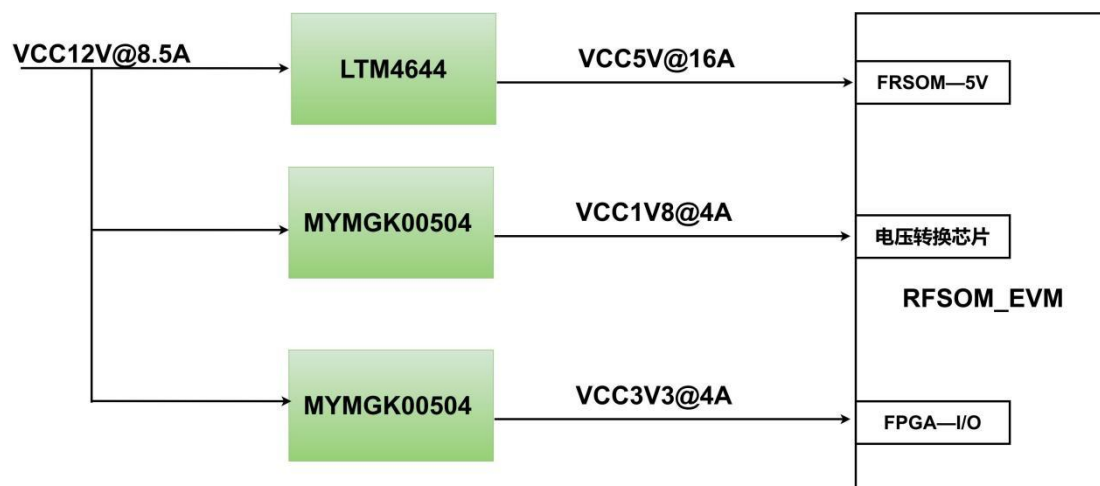


Figure 27: Power Interface Section of the RFEVM Carrier Board

### 3.12. Structural Dimensioning Diagram

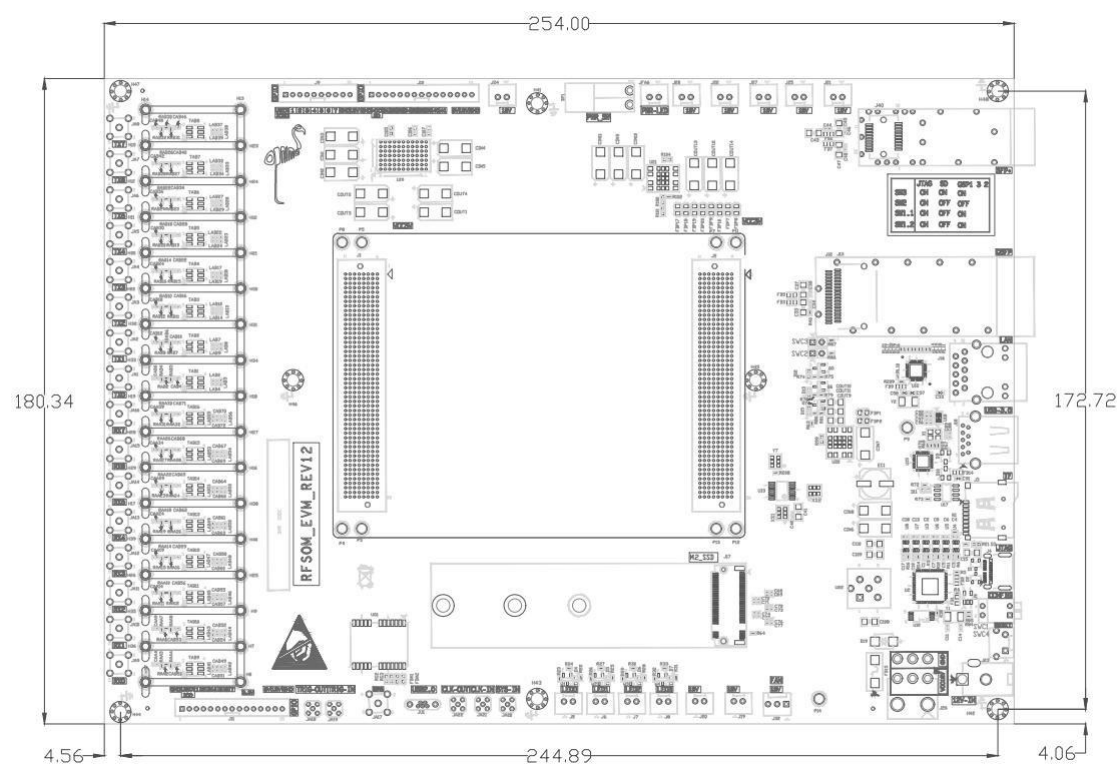


Figure 28: RFEVM Front View