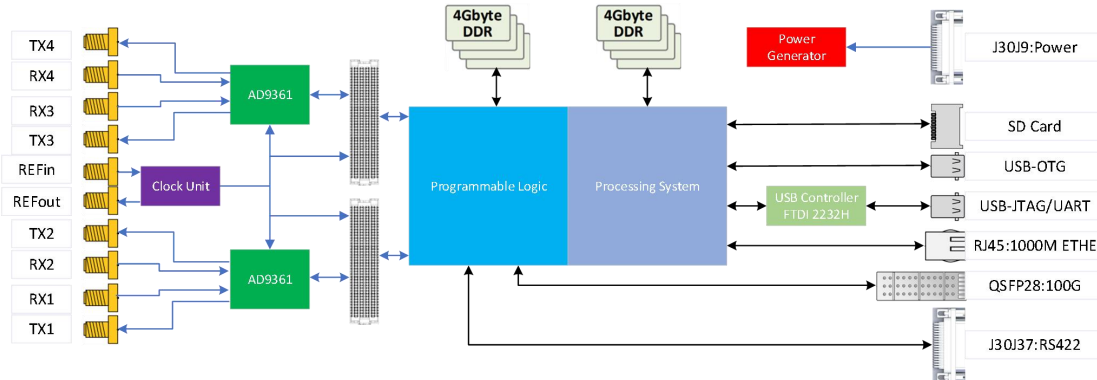


The software-defined radio processing module is designed using a "processing module + channel module" architecture in its hardware design. The processing module is based on AMD's programmable SOC processor chip, the XCZU15EG; the channel module is based on ADI's programmable transceiver RF chip, the AD9361; the two modules are interconnected via an FMC socket.



Processing Chip: xczu15eg-ffvB1156-2-I*1

RF chip: AD9361BCCZ*2

PS DDR: DDR4 4GB, 64bit/72bit

PL DDR: DDR4 4GB, 64bit

PS QSPI: 64MB

eMMC: 32GB

Clock reference input: 10 MHz, 0–10 dBm

Clock reference output: 10 MHz; AD

9361 supports baseband sampling

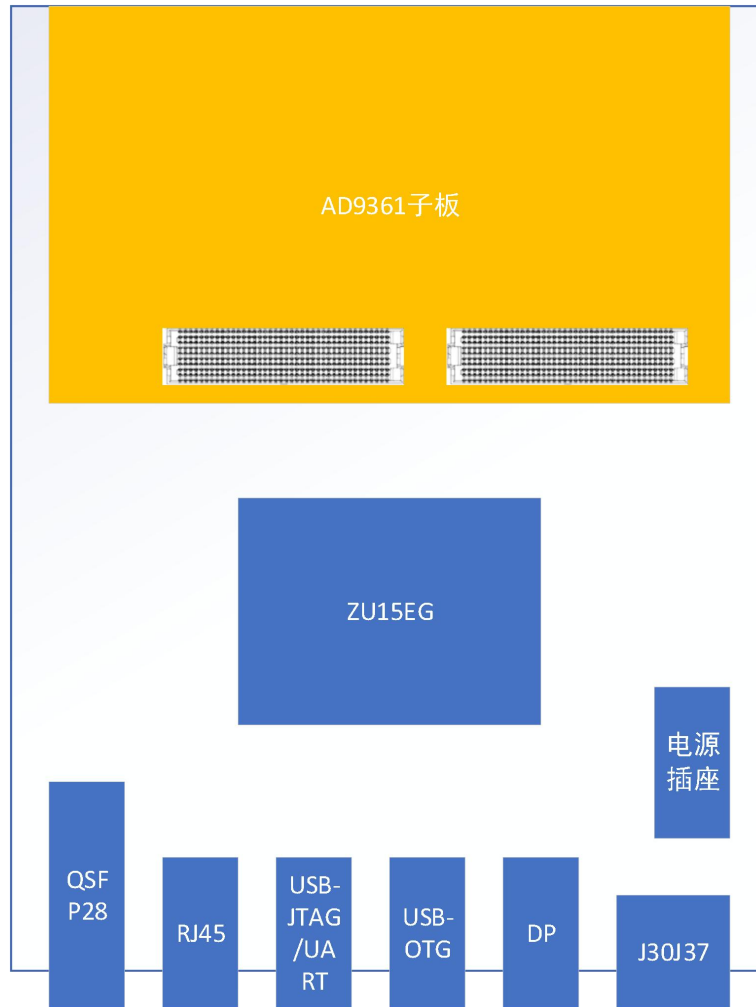
synchronization; External interfaces:

- (1) Power supply interface: DC12V (6–15V)
- (2) SD Card
- (3) USB-OTG
- (4) USB-JTAG/UART
- (5) RJ45
- (6) QSFP28*1 or SFP28*2
- (7) J30J37

Other requirements:

- (1) Processor core power supply capacity ≥ 36 A
- (2) All components are industrial-grade components, including connectors.
- (3) Suitable for operating environments ranging from -40°C to 75°C
- (4) FMC interface – Refer to the ZCU102

Module Layout Diagram



1.1.1 Processing Module Performance Requirements

- 1) Redundancy Management Chip: ADI's MAX16025 (referenced in ZCU102);
- 2) Processing chip: AMD Soc chip XCZU15EG-FFVB1156-2-I;
- 3) PS Section – DDR4: DDR4, 4 GB, 72/64-bit, 2400 MBPS;
- 4) PL Section – DDR4: DDR4, 2 GB, 32-bit, 2400 MBPS;
- 5) PS section – QSPI: 64 MB;
- 6) PS – eMMC capacity: Not less than 32 GB;
- 7) Power supply capacity: Core current ≥ 50 A (Note: PS: 10 A + PL: 40 A; refer to ZCU102 for power supply specifications);
- 8) NVMe interface: m.2;
- 9) Network interface chip: DP83867IR (referenced in ZCU102);
- 10) FMC Interface: 2 HPCs (LA+10GT; refer to ZCU102 – expand from 8GT to 10GT); Note: GTH allocation:

(1) The total 2GT from GTH228, GTH229, and GTH230 is allocated to HPC 0; the remaining 2GT from GTH230 is allocated to two SFP28 modules;

(2) All GTH129 units + all GTH130 units + 2 GTs from GTH128 are allocated to HPC1; the remaining 2 GTs from GTH128 are allocated to two SATA drives.

1.1.2 Processing Module External Interface

- 1) 10 Gigabit optical port: SFP28, 2 ports;
- 2) Gigabit Ethernet port: 1 x RJ45;
- 3) JTAG/UART debugging port: Type-C, 1 port;
- 4) USB 3.0 port: USB 3.0 (Type-C), 1 port; (GTR1)
- 5) Display interface: MiniDP – 1 port; (External GTR2 & GTR3)
- 6) RS422 interface: J30J25 – 1 pin;
- 7) USB 2.0 ports: Type-A, Hub – 4 ports (2 external, 2 internal).
- 8) Display interface: VGA (1 port; **internal**)
- 9) Hard drive interface: M.2 – 1 slot; (Internal GTR0)
- 10) Hard drive interfaces: SATA (2 ports); (GTH)
- 11) SD Card interface: TF card interface – 1; (Internal)
- 12) Power supply interfaces: 2 ports (9–36 VDC – external Type-C, internal DIP);
- 13) Internal expansion port: 1;

The processing module is depicted on the external panel as shown in Figure 2.

