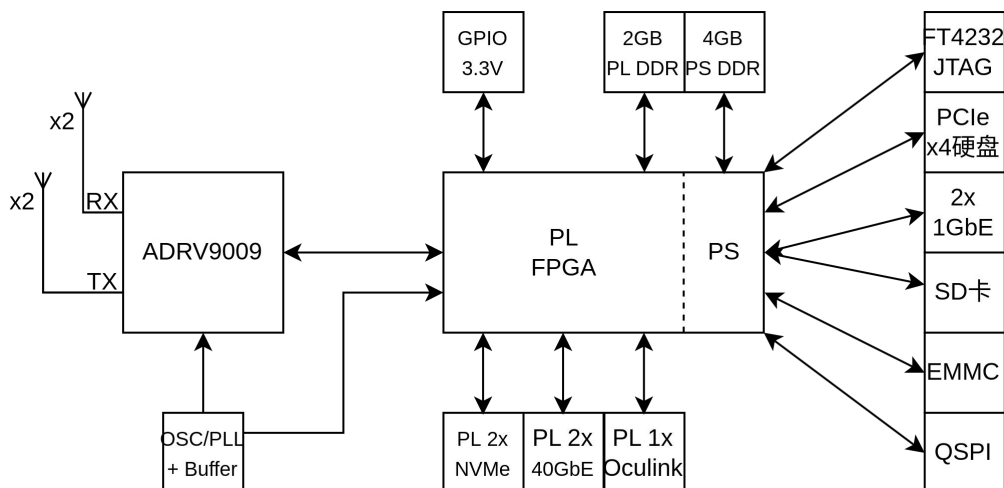


# ZU15EG SDR Board Requirements Document

## 1 Diagrammatic Sketch



## 2 Board Core Chip

- 1) FPGA: ZU15EG, 4GB PS DDR4, 2GB PL DDR4, 128MB QSPI;
- 2) Transceiver chip: 1\*ADRV9009;

## 3 Functional Performance

- 1) Supports 200 MHz bandwidth reception mode;
- 2) Supports 450 MHz bandwidth transmission mode;
- 3) The hardware supports GPIO port control for the ADRV9009-FHM functionality;
- 4) TCXO(10MHz)
- 5) Integrated 2× PS 1GBE, using GEM2/3
- 6) Built-in 1-channel, 4-configuration [Oculink](#) interface (PCIe 3.0 x4, XDMA);
- 7) Built-in two-channel, four-port 40GBASE QSFP optical fiber interfaces (UDP/RDMA);
- 8) Built-in 2-channel, 4-port NVMe interface;
- 9) Built-in EMMC (4G).

## 4 Reference Clock Requirements

- 1) The ADRV9009 Reference Clock Follows the Original Design, and the Reference Clock for the JESD204B Interface Is Synchronously Connected to the Corresponding SerDes Bank of the PL.

- 2) The PL Bank connected to NVMe uses Reference Clock 0, which shares the same crystal oscillator source as JESD204B, with a frequency of 100 MHz.
- 3) The PL Bank reference clock 0 connected to a QSFP is synchronized to the same JESD204B oscillator source, with a frequency of 156.25 MHz.
- 4) The PL Bank reference clock 1 connected to a QSFP uses a separate 156.25 MHz TCXO crystal oscillator source.
- 5) The PL Bank reference clock 0, connected to the Ocu link, shares the same crystal oscillator source as JESD204B, with a frequency of 100 MHz.
- 6) The PL Bank Reference Clock 1 connected to the OCU Link receives a 100 MHz reference clock provided by the connector (This version of the requirements document is the initial draft; the detailed clock configuration still requires further confirmation).

## 5 Interface

- 1) Power supply requirements: Must feature a wide-voltage range design (9–32 V) with reverse-connection protection functionality;
- 2) Provide at least 8 or more PL GPIOs with minimal modifications; these GPIOs must feature isolation protection functionality.
- 3) FT4232 Debugging Interface: Channel A connects to PS-JTAG; Channel B connects to any PL GPIO pin; Channel C connects to PS UART0; Channel D connects to any PL GPIO pin.
- 4) RF interface: SMP (with perforated design);

## 6 Software Requirements

- 1) Configure the ADRV9009 transceiver functionality;
- 2) Network port configuration function;
- 3) Configure DDR4 read/write operations (PS/PL);

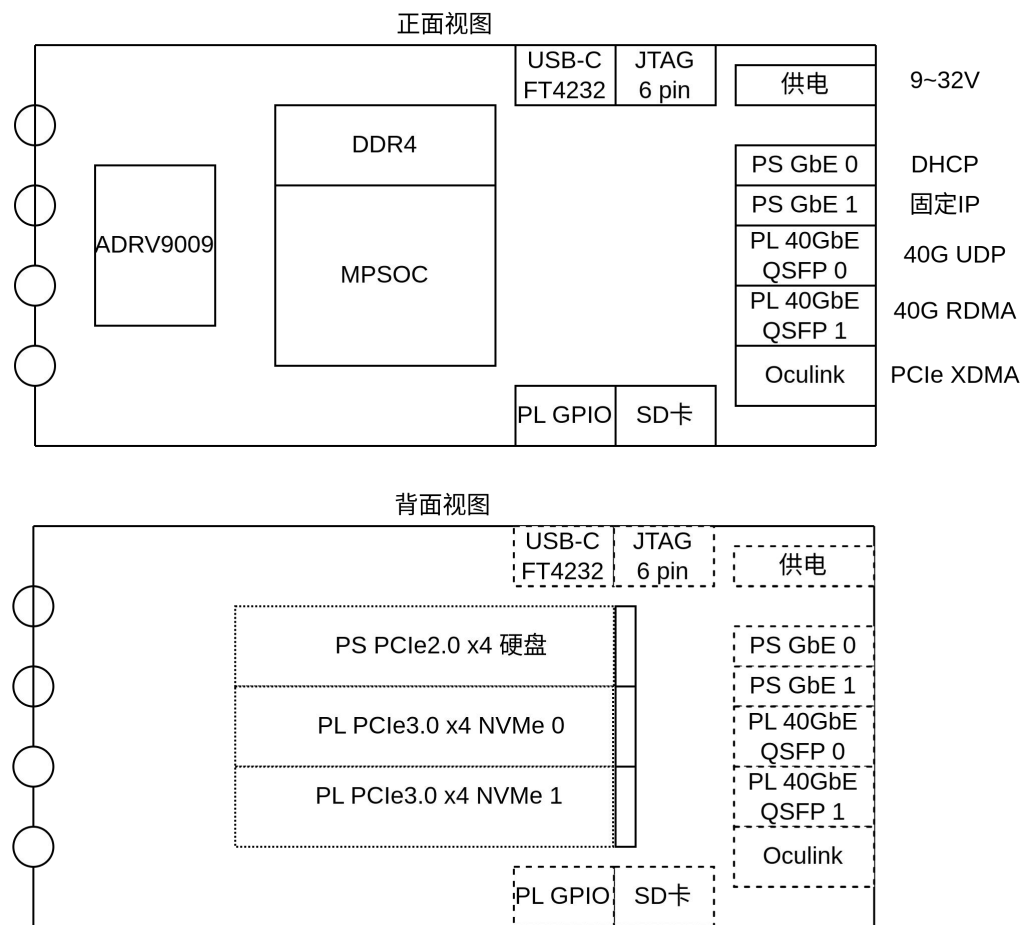
No specific software requirements apply to the SerDes interface; however, if any hardware issues are identified during the acceptance process, hardware support must be provided:

- 1) PS PCIe 2.0 x4 Hard Drive
- 2) PL XDMA/UDP/RDMA/2xNVMe

## 7 Board Specifications:

- 1) Channel isolation: >45 dBc;
- 2) 200 MHz intra-band fluctuation: <±2 dB;
- 3) No spurious dynamic range (SFDR) >50 dBc;

8 Board Layout Requirements Schematic Diagram



9 Card Cooling Method

Fanless design with integrated metal casing for heat dissipation; the hard drive bay features an open-metal-casing design. The metal casing is not included in this requirement; however, it must be coordinated with the overall casing design, including but not limited to providing necessary information such as hole locations and PCB dimensions.