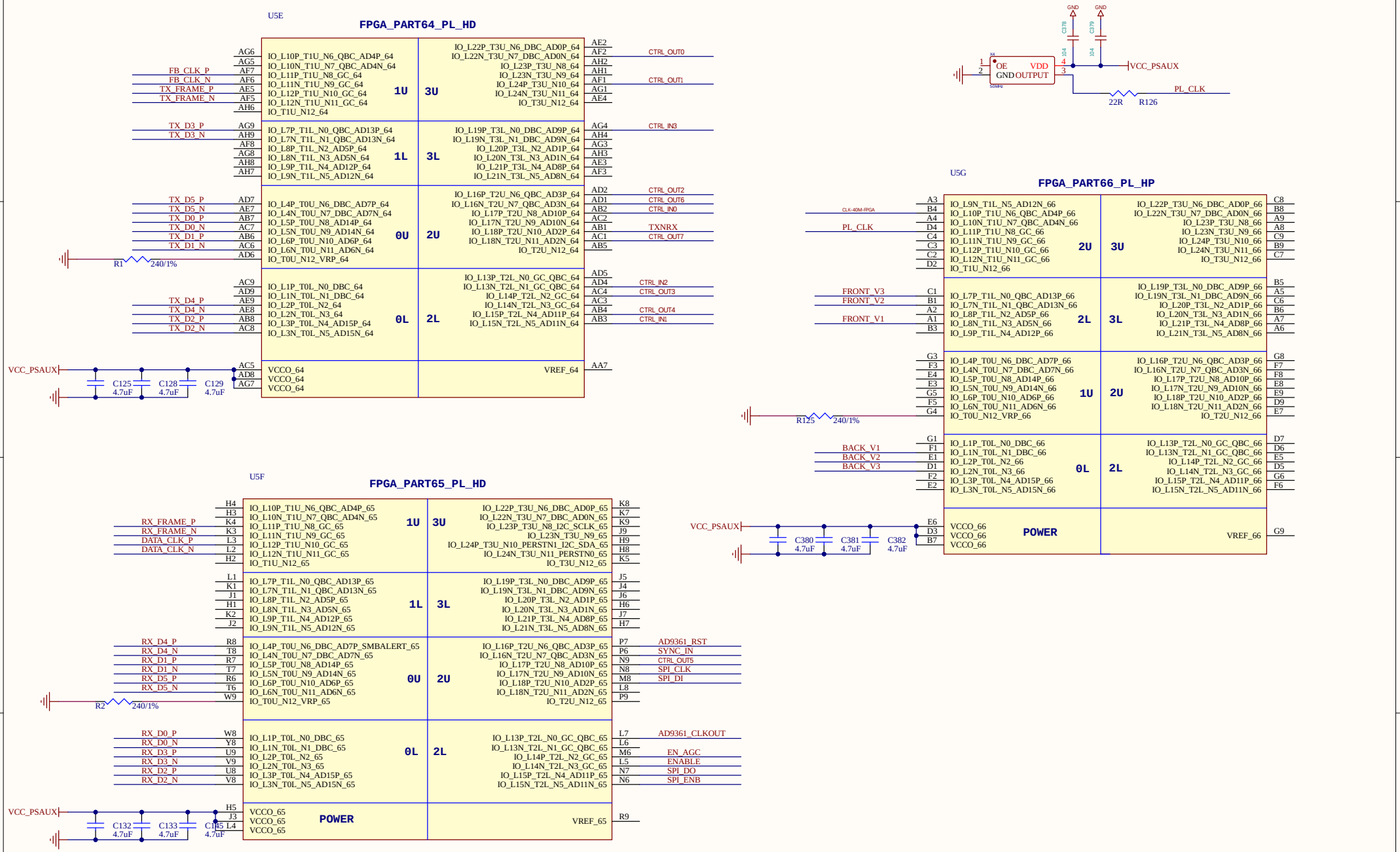
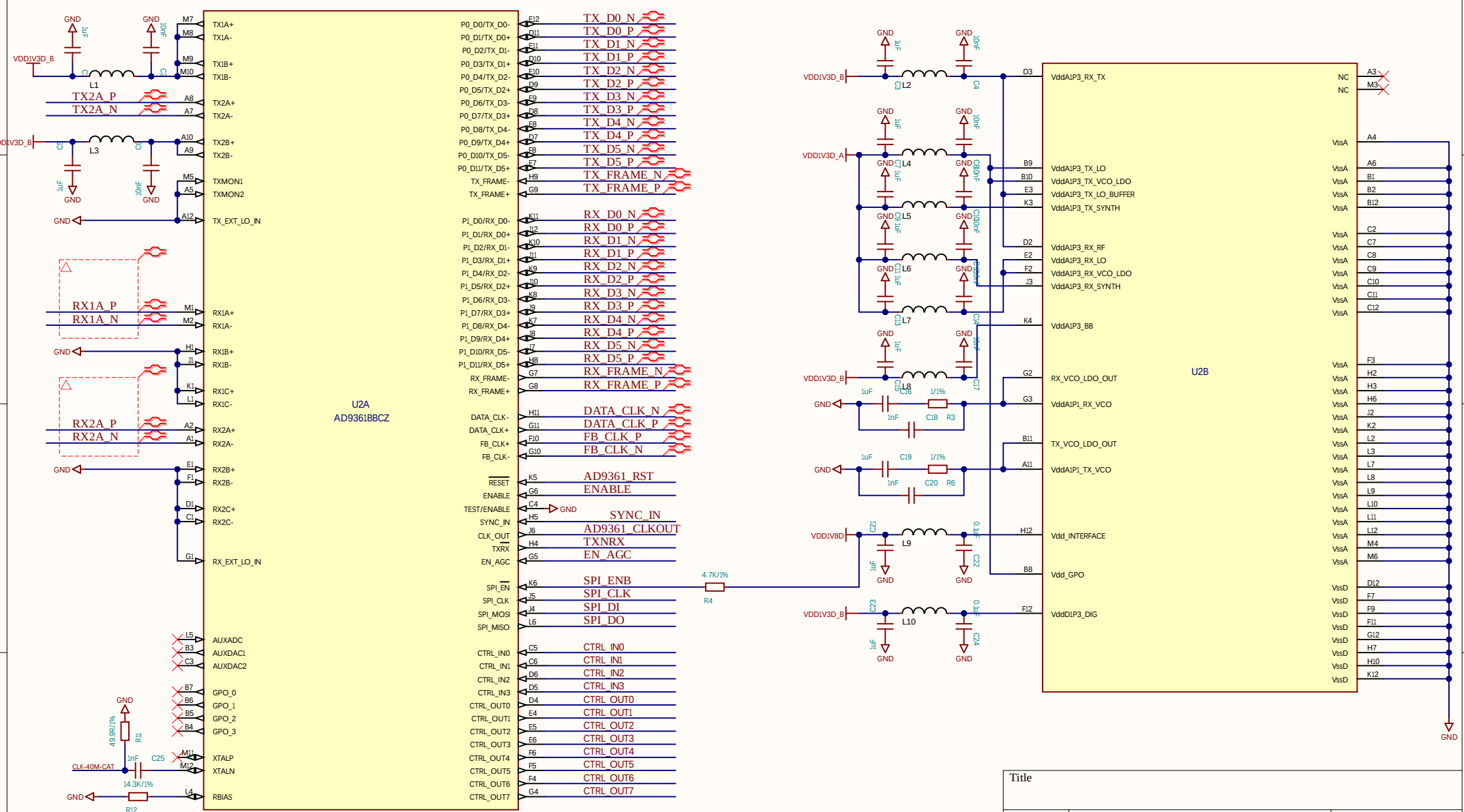
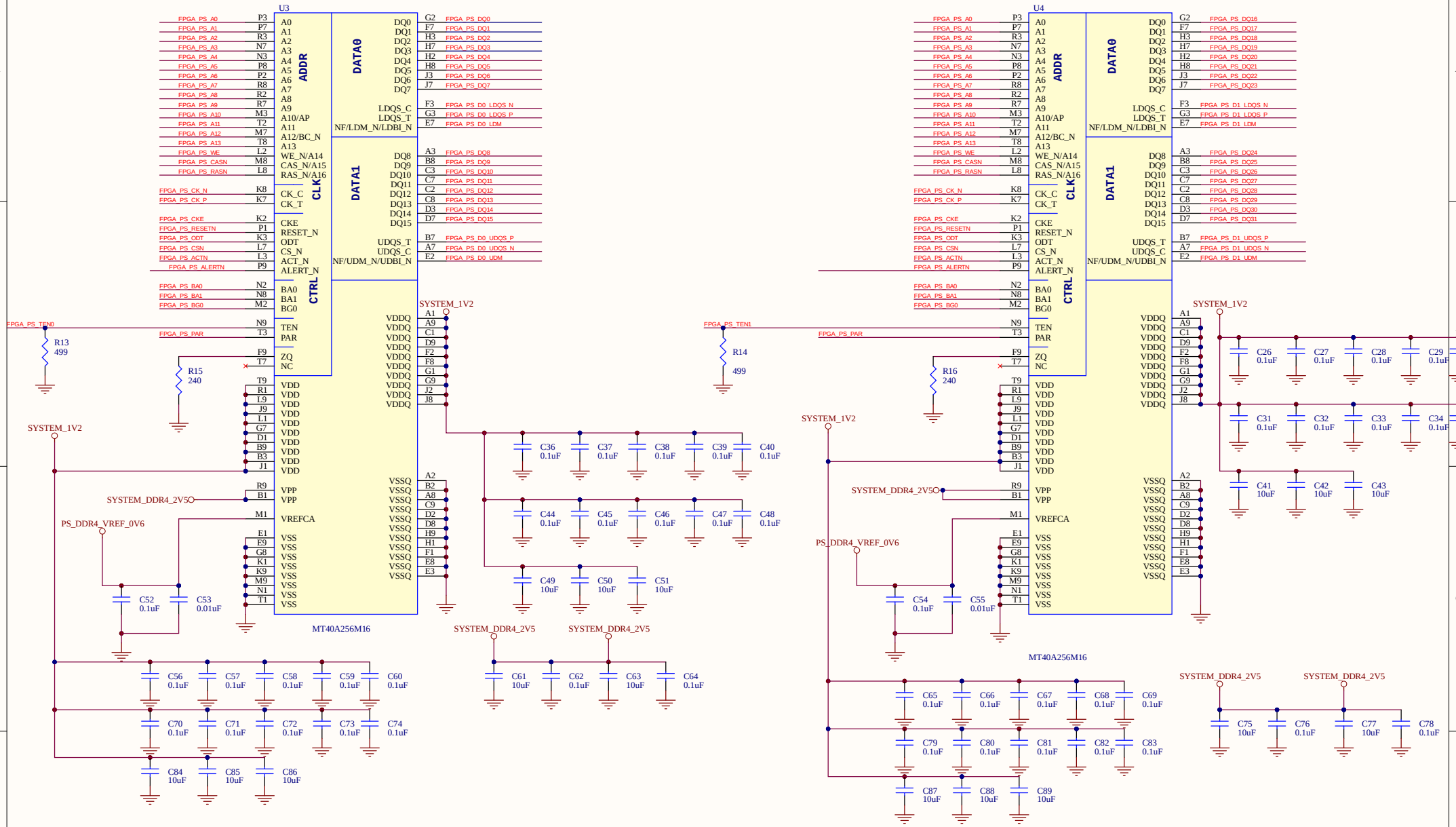
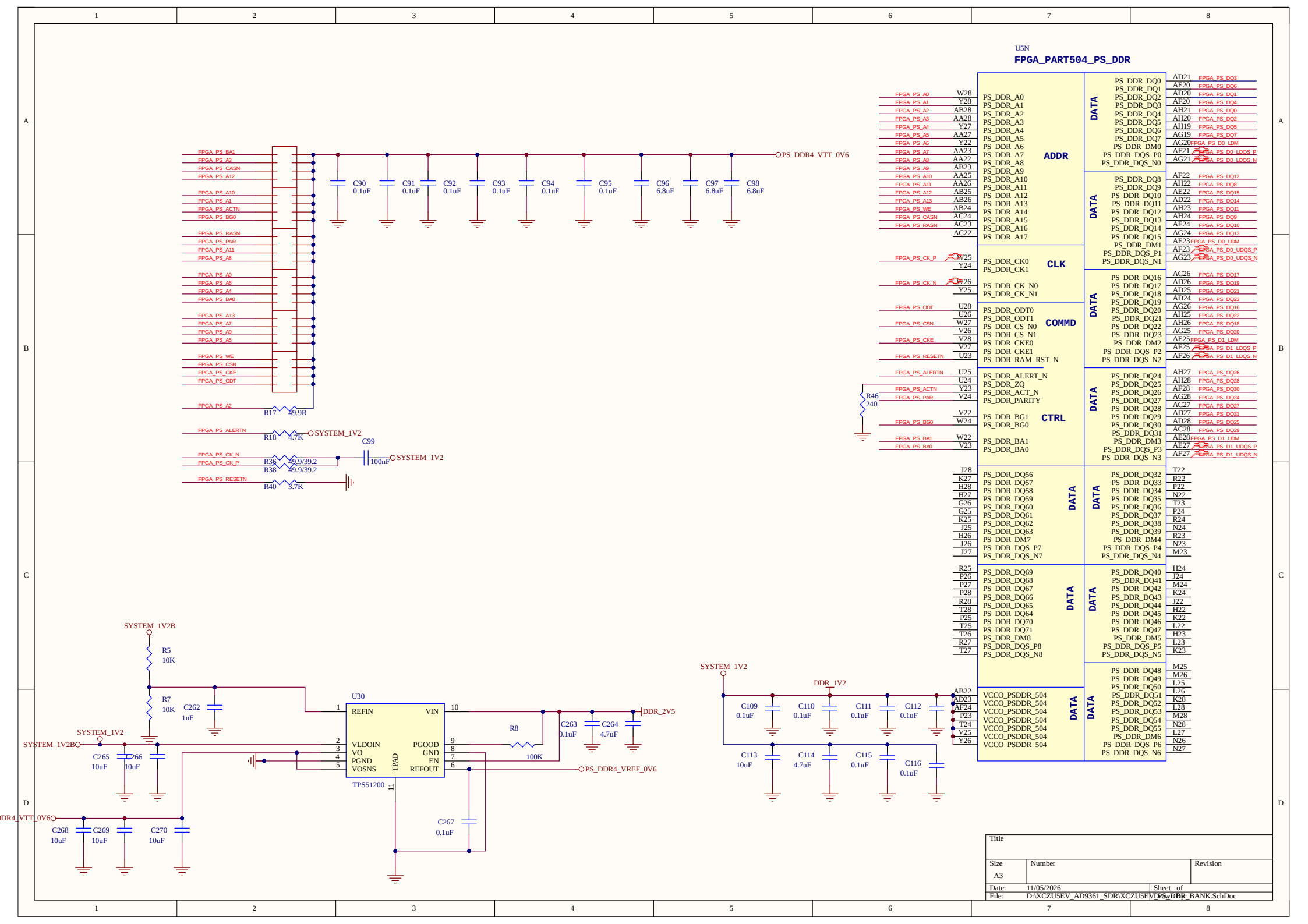

U5E
FPGA_PART64_PL_HD
1U
3U
1L
3L
0U
2U
0L
2L
POWER
VCCO_64
VREF_64
U5G
FPGA_PART66_PL_HP
U5F
FPGA_PART65_PL_HD
VCC_PSAUX
PL_CLK
22R
R126
R1
R2
R125
240/1%
C125
C128
C129
C132
C133
C135
C380
C381
C382
4.7uF
CTRL_OUT0
CTRL_OUT1
CTRL_IN3
CTRL_OUT2
CTRL_OUT6
CTRL_IN0
TXNRX
CTRL_OUT7
CTRL_IN2
CTRL_OUT3
CTRL_OUT4
CTRL_IN1
AD9361_RST
SYNC_IN
CTRL_OUT5
SPI_CLK
SPI_DI
AD9361_CLKOUT
EN_AGC
ENABLE
SPI_DO
SPI_ENB
Title
Size
A3
Number
Revision
Date:
11/05/2026
Sheet of
File:
D:\XCZU5EV_AD9361_SDR\XCZU5EV_AD9361_SDR\BANK64_65.SchDoc

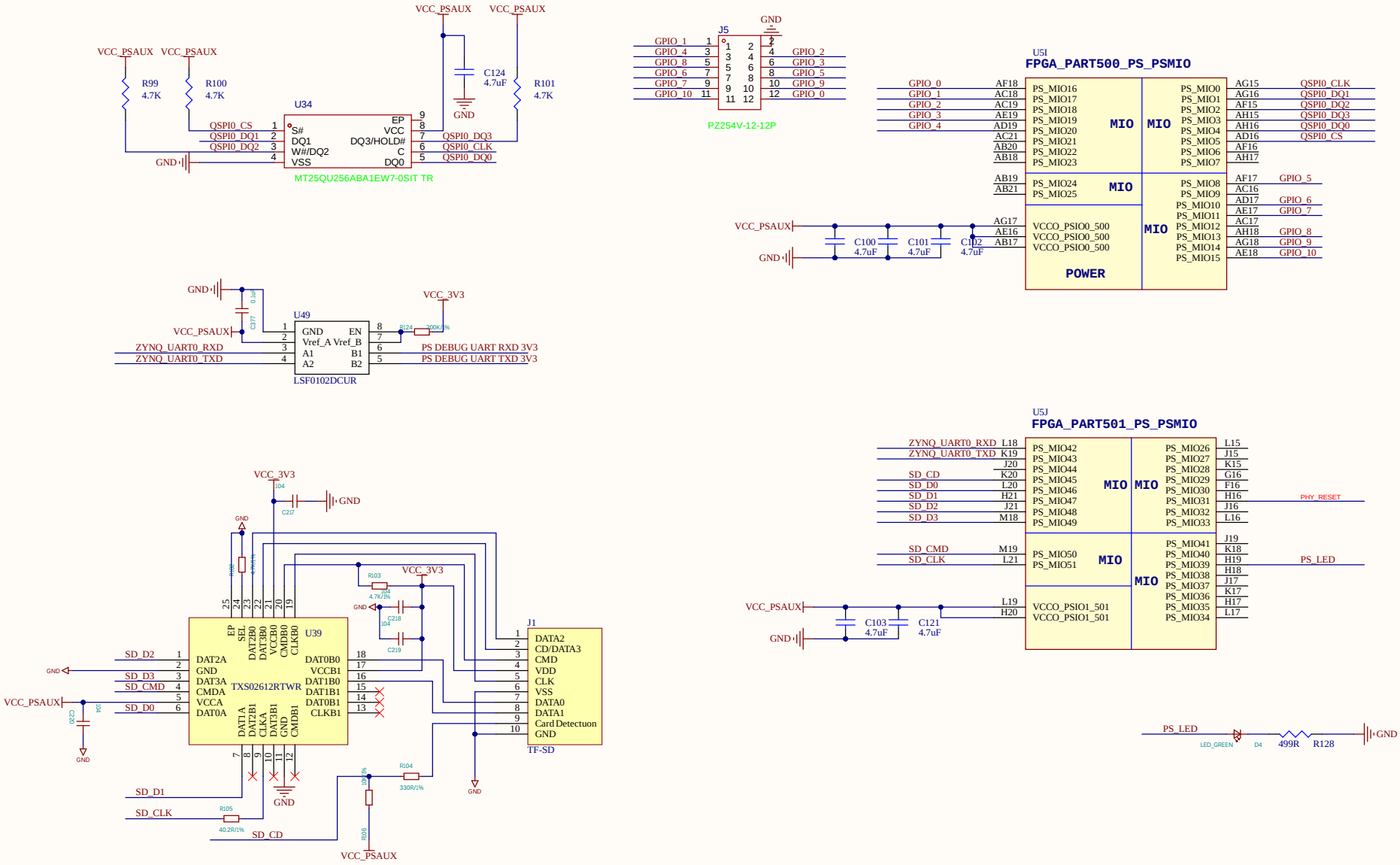


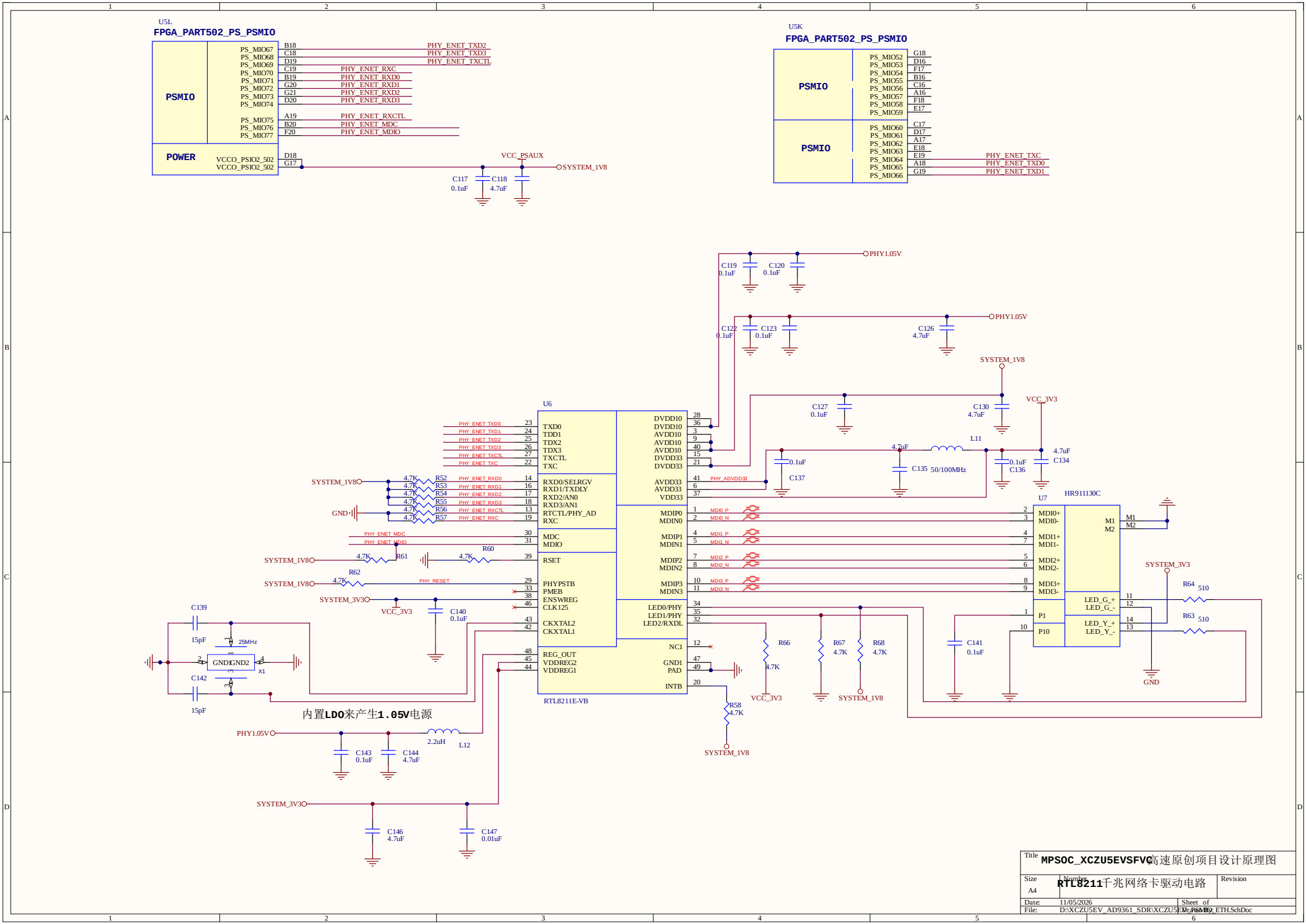
Title		
Size A4	Number	Revision
Date: 11/05/2026		Sheet of
File: D:\XCZU5EV_AD9361_SDR\AD9361_DIGITAL.SchDoc		Drawn By:



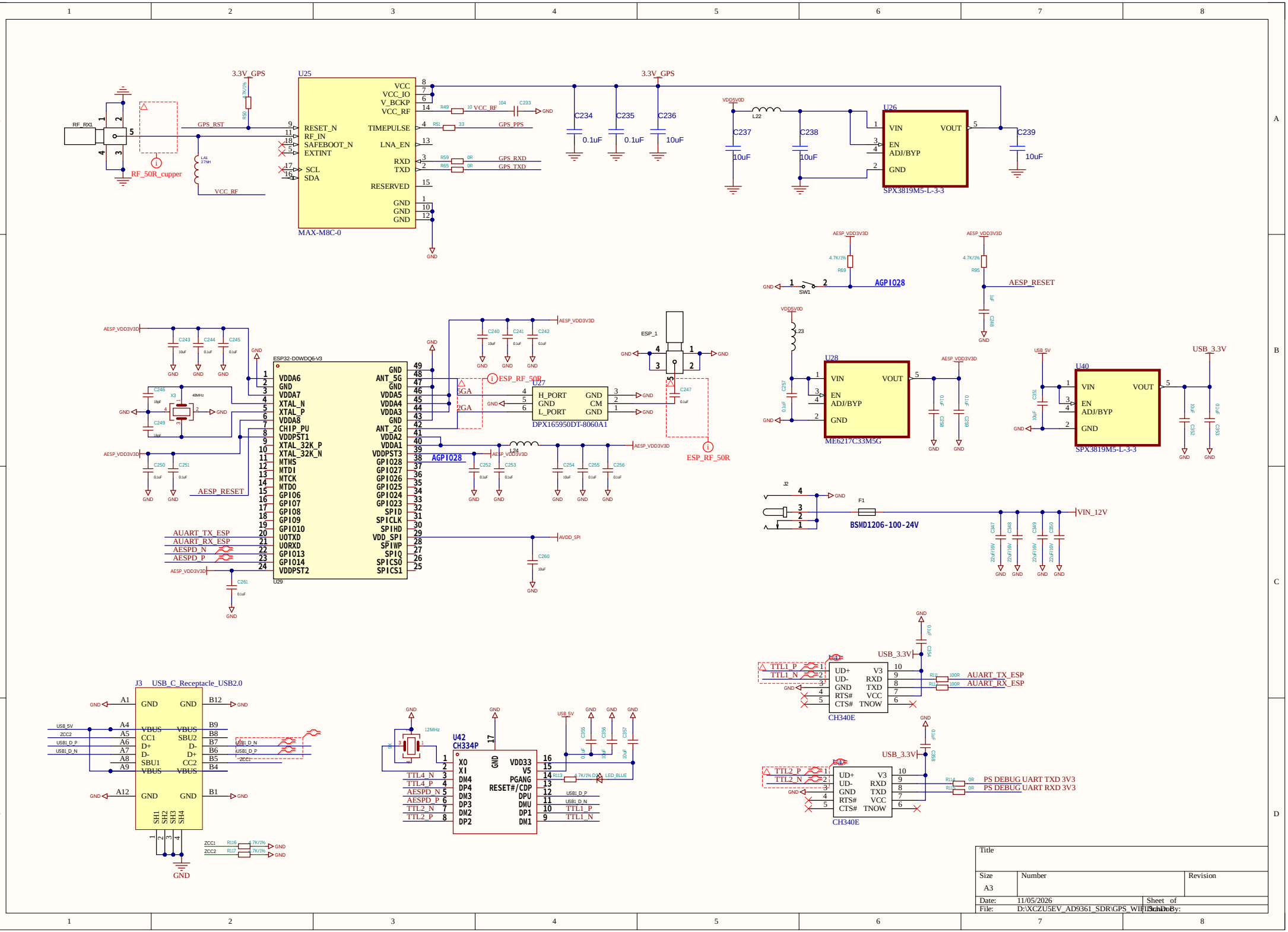
Title		
Size A3	Number	Revision
Date: 11/05/2026	Sheet of	
File: D:\XCZU5EV_AD9361_SDR\PS_DDR4_Board....	Drawn By:	


U5N
FPGA_PART504_PS_DDR
ADDR
CLK
COMMD
CTRL
DATA
PS_DDR_A0
PS_DDR_A1
PS_DDR_A2
PS_DDR_A3
PS_DDR_A4
PS_DDR_A5
PS_DDR_A6
PS_DDR_A7
PS_DDR_A8
PS_DDR_A9
PS_DDR_A10
PS_DDR_A11
PS_DDR_A12
PS_DDR_A13
PS_DDR_A14
PS_DDR_A15
PS_DDR_A16
PS_DDR_A17
PS_DDR_CK0
PS_DDR_CK1
PS_DDR_CK_N0
PS_DDR_CK_N1
PS_DDR_ODT0
PS_DDR_ODT1
PS_DDR_CS_N0
PS_DDR_CS_N1
PS_DDR_CKE0
PS_DDR_CKE1
PS_DDR_RAM_RST_N
PS_DDR_ALERT_N
PS_DDR_ZQ
PS_DDR_ACT_N
PS_DDR_PARITY
PS_DDR_BG1
PS_DDR_BG0
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DM0
PS_DDR_DQS_P0
PS_DDR_DQS_N0
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DM1
PS_DDR_DQS_P1
PS_DDR_DQS_N1
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DM2
PS_DDR_DQS_P2
PS_DDR_DQS_N2
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31
PS_DDR_DM3
PS_DDR_DQS_P3
PS_DDR_DQS_N3
PS_DDR_DQ56
PS_DDR_DQ57
PS_DDR_DQ58
PS_DDR_DQ59
PS_DDR_DQ60
PS_DDR_DQ61
PS_DDR_DQ62
PS_DDR_DQ63
PS_DDR_DM7
PS_DDR_DQS_P7
PS_DDR_DQS_N7
PS_DDR_DQ32
PS_DDR_DQ33
PS_DDR_DQ34
PS_DDR_DQ35
PS_DDR_DQ36
PS_DDR_DQ37
PS_DDR_DQ38
PS_DDR_DQ39
PS_DDR_DM4
PS_DDR_DQS_P4
PS_DDR_DQS_N4
PS_DDR_DQ69
PS_DDR_DQ68
PS_DDR_DQ67
PS_DDR_DQ66
PS_DDR_DQ65
PS_DDR_DQ64
PS_DDR_DQ70
PS_DDR_DQ71
PS_DDR_DM8
PS_DDR_DQS_P8
PS_DDR_DQS_N8
PS_DDR_DQ40
PS_DDR_DQ41
PS_DDR_DQ42
PS_DDR_DQ43
PS_DDR_DQ44
PS_DDR_DQ45
PS_DDR_DQ46
PS_DDR_DQ47
PS_DDR_DM5
PS_DDR_DQS_P5
PS_DDR_DQS_N5
VCCO_PSDDR_504
PS_DDR_DQ48
PS_DDR_DQ49
PS_DDR_DQ50
PS_DDR_DQ51
PS_DDR_DQ52
PS_DDR_DQ53
PS_DDR_DQ54
PS_DDR_DQ55
PS_DDR_DM6
PS_DDR_DQS_P6
PS_DDR_DQS_N6
FPGA_PS_A0
FPGA_PS_A1
FPGA_PS_A2
FPGA_PS_A3
FPGA_PS_A4
FPGA_PS_A5
FPGA_PS_A6
FPGA_PS_A7
FPGA_PS_A8
FPGA_PS_A9
FPGA_PS_A10
FPGA_PS_A11
FPGA_PS_A12
FPGA_PS_A13
FPGA_PS_WE
FPGA_PS_CASN
FPGA_PS_RASN
FPGA_PS_CK_P
FPGA_PS_CK_N
FPGA_PS_ODT
FPGA_PS_CSN
FPGA_PS_CKE
FPGA_PS_RESETN
FPGA_PS_ALERTN
FPGA_PS_ACTN
FPGA_PS_PAR
FPGA_PS_BG0
FPGA_PS_BA1
FPGA_PS_BA0
FPGA_PS_DQ0
FPGA_PS_DQ1
FPGA_PS_DQ2
FPGA_PS_DQ3
FPGA_PS_DQ4
FPGA_PS_DQ5
FPGA_PS_DQ6
FPGA_PS_DQ7
FPGA_PS_D0_LDM
FPGA_PS_D0_LDQS_P
FPGA_PS_D0_LDQS_N
FPGA_PS_DQ8
FPGA_PS_DQ9
FPGA_PS_DQ10
FPGA_PS_DQ11
FPGA_PS_DQ12
FPGA_PS_DQ13
FPGA_PS_DQ14
FPGA_PS_DQ15
FPGA_PS_D0_UDM
FPGA_PS_D0_UDQS_P
FPGA_PS_D0_UDQS_N
FPGA_PS_DQ16
FPGA_PS_DQ17
FPGA_PS_DQ18
FPGA_PS_DQ19
FPGA_PS_DQ20
FPGA_PS_DQ21
FPGA_PS_DQ22
FPGA_PS_DQ23
FPGA_PS_D1_LDM
FPGA_PS_D1_LDQS_P
FPGA_PS_D1_LDQS_N
FPGA_PS_DQ24
FPGA_PS_DQ25
FPGA_PS_DQ26
FPGA_PS_DQ27
FPGA_PS_DQ28
FPGA_PS_DQ29
FPGA_PS_DQ30
FPGA_PS_DQ31
FPGA_PS_D1_UDM
FPGA_PS_D1_UDQS_P
FPGA_PS_D1_UDQS_N
R46 240
C90 0.1uF
C91 0.1uF
C92 0.1uF
C93 0.1uF
C94 0.1uF
C95 0.1uF
C96 6.8uF
C97 6.8uF
C98 6.8uF
PS_DDR4_VTT_0V6
R17 49.9R
R18 4.7K
SYSTEM_1V2
C99 100nF
R36 49.9/39.2
R38 49.9/39.2
R40 3.7K
SYSTEM_1V2B
R5 10K
R7 10K
C262 1nF
U30
REFIN
VIN
VLDOIN
VO
PGND
VOSNS
TPAD
PGOOD
GND
EN
REFOUT
TPS51200
R8 100K
C263 0.1uF
C264 4.7uF
DDR_2V5
PS_DDR4_VREF_0V6
C265 10uF
C266 10uF
C267 0.1uF
C268 10uF
C269 10uF
C270 10uF
DDR_1V2
C109 0.1uF
C110 0.1uF
C111 0.1uF
C112 0.1uF
C113 10uF
C114 4.7uF
C115 0.1uF
C116 0.1uF
Title
Size A3
Number
Revision
Date: 11/05/2026
Sheet of
File: D:\XCZU5EV_AD9361_SDR\XCZU5EV_PS_DDR_BANK.SchDoc

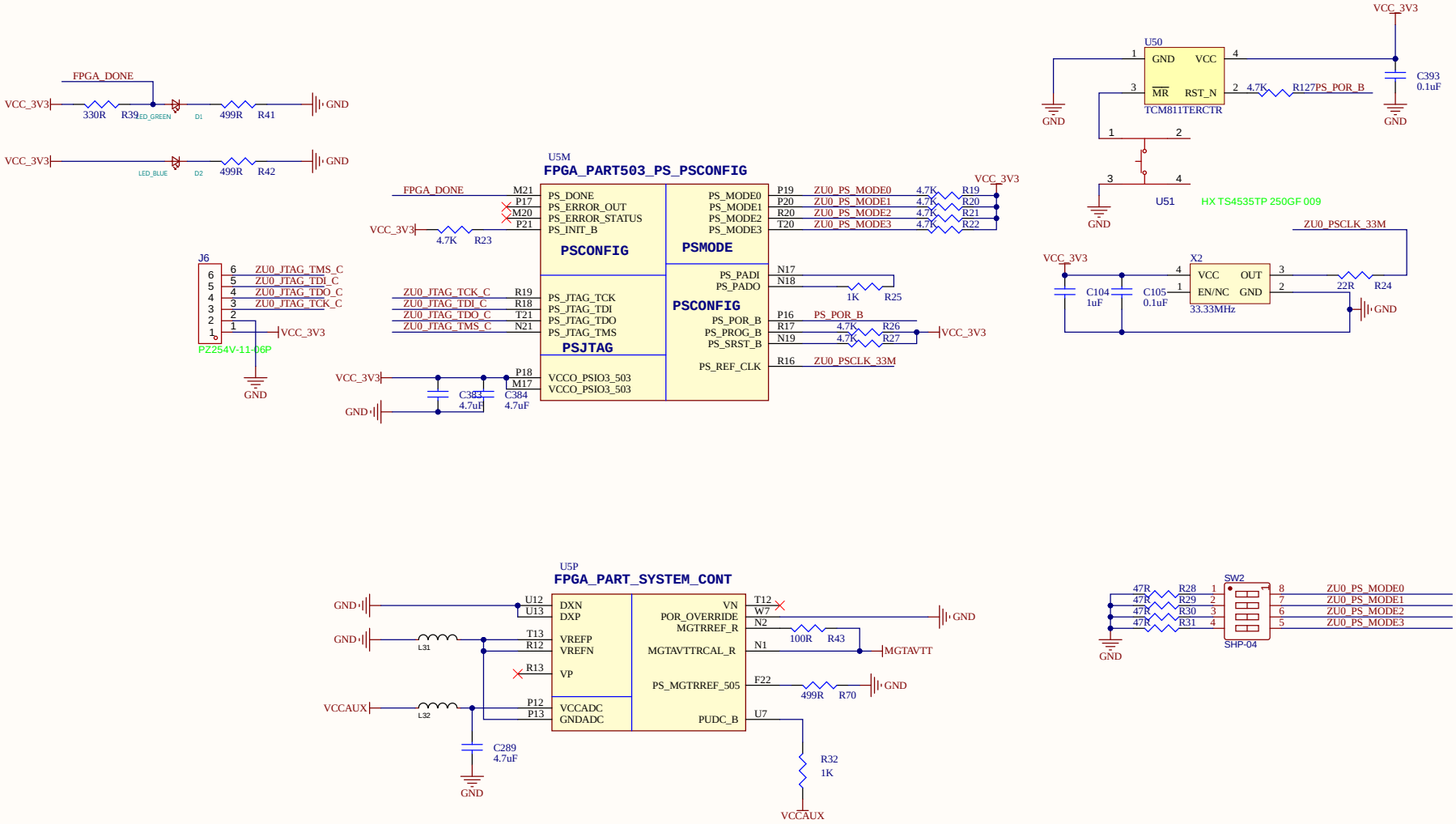

VCC_PSAUX
VCC_PSAUX
R99
4.7K
R100
4.7K
U34
QSPI0_CS
QSPI0_DQ1
QSPI0_DQ2
GND
S#
DQ1
W#/DQ2
VSS
EP
VCC
DQ3/HOLD#
C
DQ0
QSPI0_DQ3
QSPI0_CLK
QSPI0_DQ0
C124
4.7uF
R101
4.7K
MT25QU256ABA1EW7-0SIT TR
J5
GPIO_1
GPIO_4
GPIO_8
GPIO_6
GPIO_7
GPIO_10
GPIO_2
GPIO_3
GPIO_5
GPIO_9
GPIO_0
PZ254V-12-12P
U5I
FPGA_PART500_PS_PSMIO
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
PS_MIO16
PS_MIO17
PS_MIO18
PS_MIO19
PS_MIO20
PS_MIO21
PS_MIO22
PS_MIO23
PS_MIO24
PS_MIO25
VCCO_PSIO0_500
VCCO_PSIO0_500
VCCO_PSIO0_500
POWER
MIO
PS_MIO0
PS_MIO1
PS_MIO2
PS_MIO3
PS_MIO4
PS_MIO5
PS_MIO6
PS_MIO7
PS_MIO8
PS_MIO9
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
PS_MIO14
PS_MIO15
QSPI0_CLK
QSPI0_DQ1
QSPI0_DQ2
QSPI0_DQ3
QSPI0_DQ0
QSPI0_CS
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
C100
4.7uF
C101
4.7uF
C102
4.7uF
GND
VCC_PSAUX
GND
C377
0.1uF
U49
VCC_3V3
VCC_PSAUX
ZYNQ_UART0_RXD
ZYNQ_UART0_TXD
GND
EN
Vref_A
Vref_B
A1
A2
B1
B2
R124
200K/1%
PS DEBUG UART RXD 3V3
PS DEBUG UART TXD 3V3
LSF0102DCUR
U5J
FPGA_PART501_PS_PSMIO
ZYNQ_UART0_RXD
ZYNQ_UART0_TXD
SD_CD
SD_D0
SD_D1
SD_D2
SD_D3
SD_CMD
SD_CLK
PS_MIO42
PS_MIO43
PS_MIO44
PS_MIO45
PS_MIO46
PS_MIO47
PS_MIO48
PS_MIO49
PS_MIO50
PS_MIO51
VCCO_PSIO1_501
VCCO_PSIO1_501
MIO
PS_MIO26
PS_MIO27
PS_MIO28
PS_MIO29
PS_MIO30
PS_MIO31
PS_MIO32
PS_MIO33
PS_MIO41
PS_MIO40
PS_MIO39
PS_MIO38
PS_MIO37
PS_MIO36
PS_MIO35
PS_MIO34
PHY_RESET
PS_LED
C103
4.7uF
C121
4.7uF
VCC_PSAUX
GND
VCC_3V3
GND
C217
104
R102
4.7K/1%
R103
4.7K/1%
C218
104
C219
104
C221
104
U39
TXS02612RTWR
EP
SEL
DAT2B0
DAT3B0
VCCB0
CMDB0
CLKB0
DAT2A
GND
DAT3A
CMDA
VCCA
DAT0A
DAT0B0
VCCB1
DAT1B0
DAT1B1
DAT0B1
CLKB1
DAT1A
DAT2B1
CLKA
DAT3B1
GND
CMDB1
J1
DATA2
CD/DATA3
CMD
VDD
CLK
VSS
DATA0
DATA1
Card Detectuon
GND
TF-SD
SD_D1
SD_CLK
SD_CD
R105
40.2R/1%
R104
330R/1%
R106
10K/1%
PS_LED
LED_GREEN
D4
499R
R128
GND
Title
Size
A3
Number
Revision
Date:
11/05/2026
Sheet of
File:
D:\XCZU5EV_AD9361_SDR\XCZU5EV_PSMIO_QSPI_SD.SchDoc



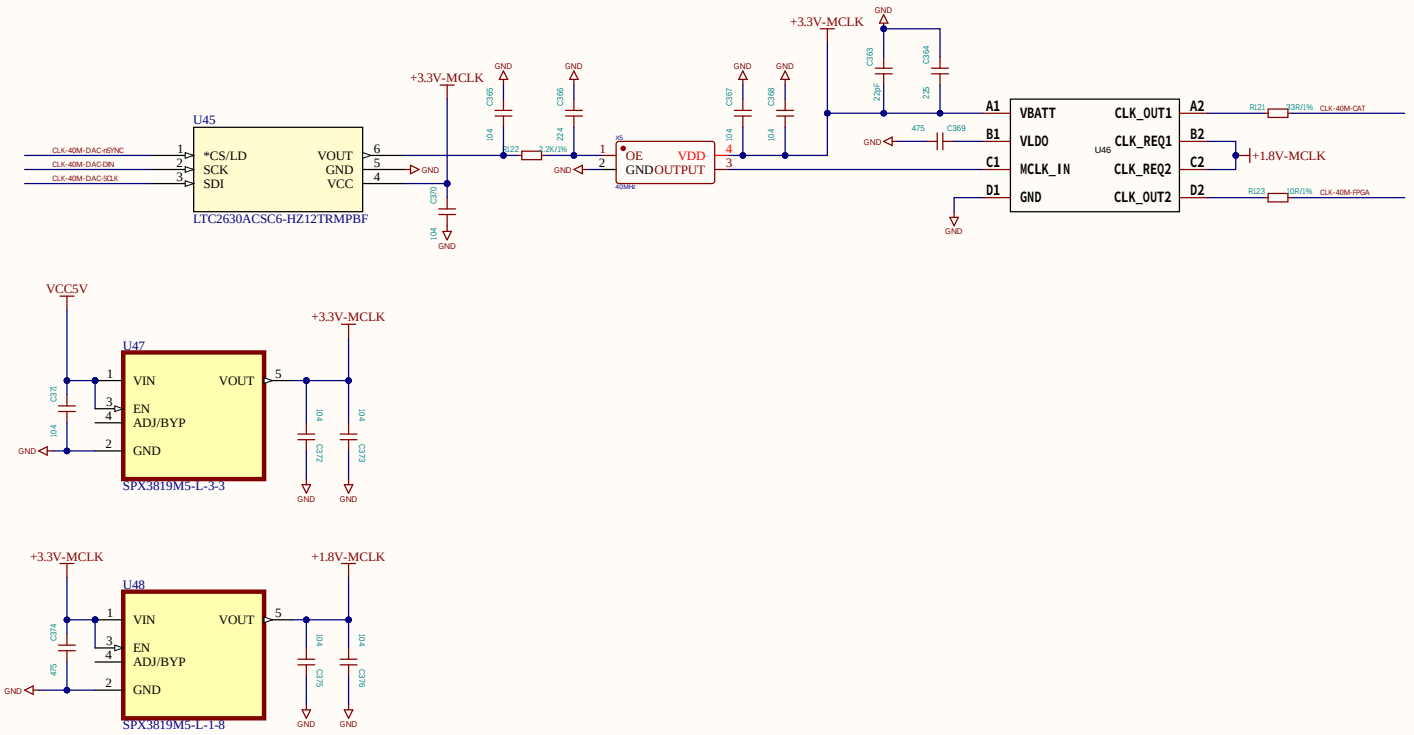
U5L
FPGA_PART502_PS_PSMIO
PSMIO
POWER
PS_MIO67 B18 PHY_ENET_TXD2
PS_MIO68 C18 PHY_ENET_TXD3
PS_MIO69 D19 PHY_ENET_TXCTL
PS_MIO70 C19 PHY_ENET_RXC
PS_MIO71 B19 PHY_ENET_RXD0
PS_MIO72 G20 PHY_ENET_RXD1
PS_MIO73 G21 PHY_ENET_RXD2
PS_MIO74 D20 PHY_ENET_RXD3
PS_MIO75 A19 PHY_ENET_RXCTL
PS_MIO76 B20 PHY_ENET_MDC
PS_MIO77 F20 PHY_ENET_MDIO
VCCO_PSIO2_502 D18
VCCO_PSIO2_502 G17
VCC_PSAUX
SYSTEM_1V8
C117 0.1uF
C118 4.7uF
U5K
FPGA_PART502_PS_PSMIO
PSMIO
PSMIO
PS_MIO52 G18
PS_MIO53 D16
PS_MIO54 F17
PS_MIO55 B16
PS_MIO56 C16
PS_MIO57 A16
PS_MIO58 F18
PS_MIO59 E17
PS_MIO60 C17
PS_MIO61 D17
PS_MIO62 A17
PS_MIO63 E18
PS_MIO64 E19 PHY_ENET_TXC
PS_MIO65 A18 PHY_ENET_TXD0
PS_MIO66 G19 PHY_ENET_TXD1
PHY1.05V
C119 0.1uF
C120 0.1uF
C122 0.1uF
C123 0.1uF
C126 4.7uF
SYSTEM_1V8
C127 0.1uF
C130 4.7uF
VCC_3V3
L11
4.7uF
C135 50/100MHz
0.1uF C136
4.7uF C134
0.1uF C137
PHY_ADVDD33
U6
RTL8211E-VB
TXD0 TDD1 TDX2 TDX3 TXCTL TXC
RXD0/SELRGV RXD1/TXDLY RXD2/AN0 RXD3/AN1 RTCTL/PHY_AD RXC
MDC MDIO
RSET
PHYPSTB PMEB ENSWREG CLK125
CKXTAL2 CKXTAL1
REG_OUT VDDREG2 VDDREG1
DVDD10 DVDD10 AVDD10 AVDD10 AVDD10 DVDD33 DVDD33
AVDD33 AVDD33 VDD33
MDIP0 MDIN0
MDIP1 MDIN1
MDIP2 MDIN2
MDIP3 MDIN3
LED0/PHY LED1/PHY LED2/RXDL
NC1
GND1 PAD
INTB
PHY_ENET_TXD0 PHY_ENET_TXD1 PHY_ENET_TXD2 PHY_ENET_TXD3 PHY_ENET_TXCTL PHY_ENET_TXC
PHY_ENET_RXD0 PHY_ENET_RXD1 PHY_ENET_RXD2 PHY_ENET_RXD3 PHY_ENET_RXCTL PHY_ENET_RXC
PHY_ENET_MDC PHY_ENET_MDIO
PHY_RESET
SYSTEM_1V8
GND
4.7K R52 R53 R54 R55 R56 R57
4.7K R61
R60 4.7K
R62 4.7K
SYSTEM_3V3
VCC_3V3
C140 0.1uF
C139 15pF
25MHz
GND1 GND2 X1
C142 15pF
内置LDO来产生1.05V电源
PHY1.05V
C143 0.1uF
C144 4.7uF
2.2uH L12
SYSTEM_3V3
C146 4.7uF
C147 0.01uF
MDI0_P MDI0_N MDI1_P MDI1_N MDI2_P MDI2_N MDI3_P MDI3_N
R66 4.7K
R67 4.7K
R68 4.7K
R58 4.7K
VCC_3V3
SYSTEM_1V8
U7
HR911130C
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
P1 P10
M1 M2
LED_G_+ LED_G_-
LED_Y_+ LED_Y_-
C141 0.1uF
SYSTEM_3V3
R64 510
R63 510
GND
Title MPSOC_XCZU5EVSFVC高速原创项目设计原理图
Size A4
Number RTL8211千兆网络卡驱动电路
Revision
Date: 11/05/2026
Sheet of
File: D:\XCZU5EV_AD9361_SDR\XCZU5EV_PSMIO_ETH.SchDoc
Drawn By:



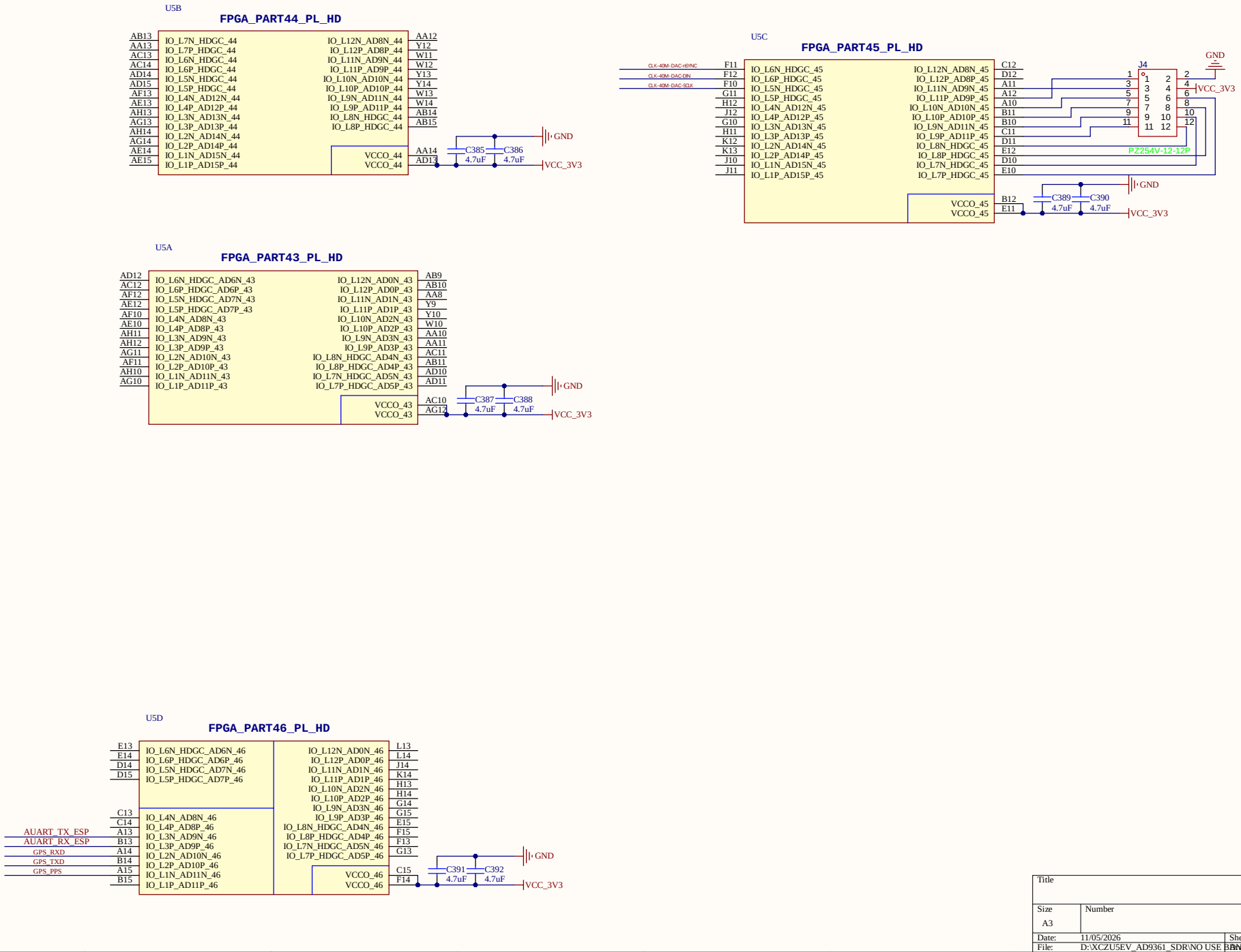
U25
MAX-M8C-0
RESET_N
RF_IN
SAFEBOOT_N
EXTINT
SCL
SDA
VCC
VCC_IO
V_BCKP
VCC_RF
TIMEPULSE
LNA_EN
RXD
TXD
RESERVED
GND
3.3V_GPS
GPS_RST
GPS_PPS
GPS_RXD
GPS_TXD
RF_RX1
RF_50R_cupper
VCC_RF
C234
C235
C236
0.1uF
10uF
C237
C238
C239
U26
SPX3819M5-L-3-3
VIN
VOUT
EN
ADJ/BYP
AGPIO28
AESP_RESET
U28
ME6217C33M5G
U40
SPX3819M5-L-3-3
USB_3.3V
ESP32-D0WDQ6-V3
U29
VDDA6
VDDA7
XTAL_N
XTAL_P
VDDA8
CHIP_PU
VDDPST1
XTAL_32K_P
XTAL_32K_N
MTMS
MTDI
MTCK
MTDO
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
UOTXD
UORXD
GPIO13
GPIO14
VDDPST2
ANT_5G
VDDA5
VDDA4
VDDA3
ANT_2G
VDDA2
VDDA1
VDDPST3
GPIO28
GPIO27
GPIO26
GPIO25
GPIO24
GPIO23
SPID
SPICLK
SPIHD
VDD_SPI
SPIWP
SPIQ
SPICS0
SPICS1
AUART_TX_ESP
AUART_RX_ESP
AESPD_N
AESPD_P
ESP_RF_50R
U27
DPX165950DT-8060A1
H_PORT
L_PORT
CM
ESP_1
J2
BSMD1206-100-24V
VIN_12V
J3
USB_C_Receptacle_USB2.0
GND
VBUS
CC1
D+
D-
SBU1
SBU2
CC2
SH1
SH2
SH3
SH4
U42
CH334P
XO
XI
DM4
DP4
DM3
DP3
DM2
DP2
VDD33
V5
PGANG
RESET#/CDP
DPU
DMU
DP1
DM1
TTL4_N
TTL4_P
AESPD_N
AESPD_P
TTL2_N
TTL2_P
TTL1_P
TTL1_N
LED_BLUE
CH340E
UD+
UD-
RTS#
CTS#
V3
RXD
TXD
VCC
TNOW
PS DEBUG UART TXD 3V3
PS DEBUG UART RXD 3V3
Title
Size
A3
Number
Revision
Date: 11/05/2026
Sheet of
File: D:\XCZU5EV_AD9361_SDR\GPS_WIFI.PrjPcb
Drawn By:

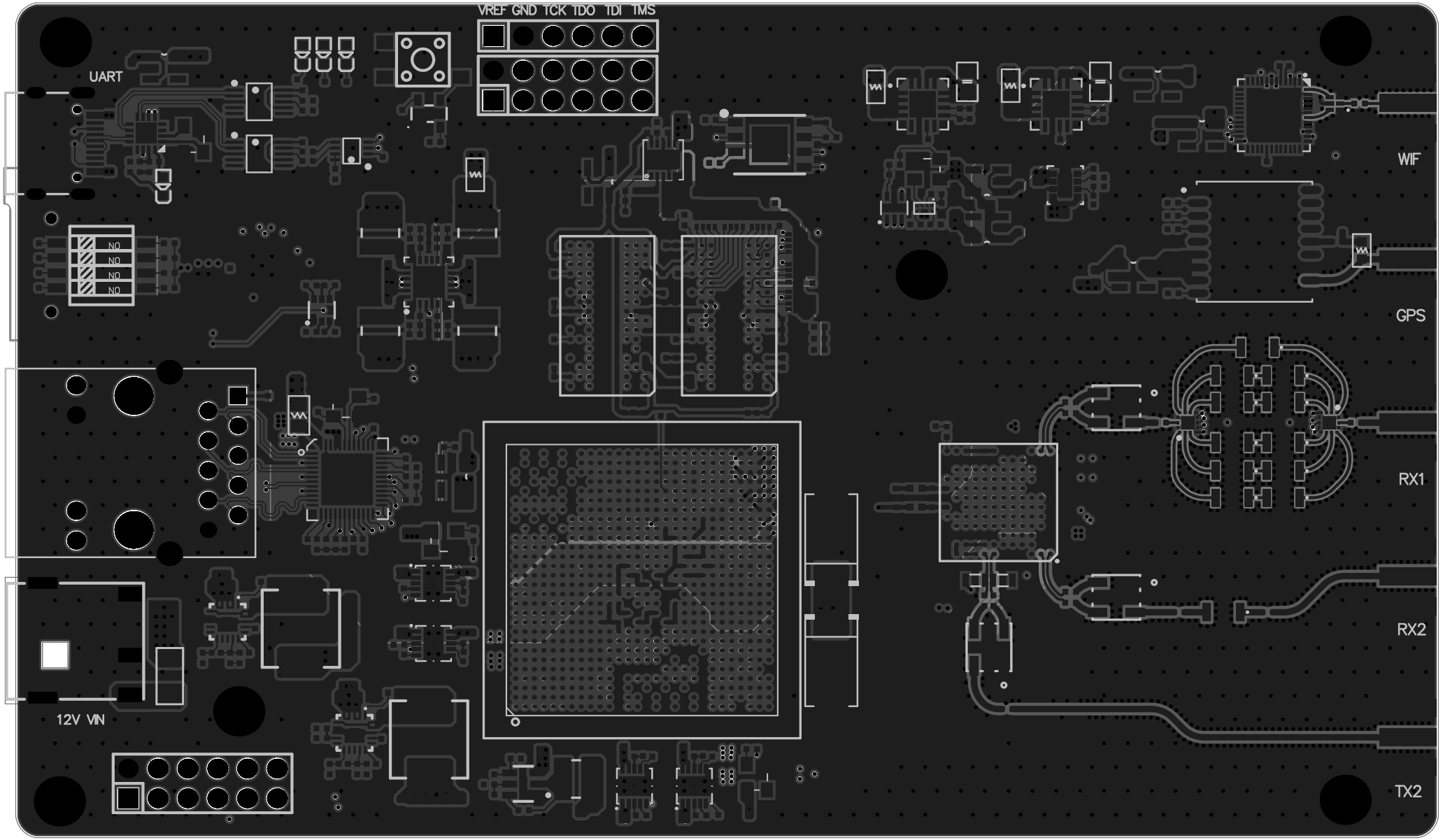


Title		
Size A3	Number	Revision
Date: 11/05/2026	Sheet of	
File: D:\XCZU5EV_AD9361_SDR\XCZU5EV_PSMIO_CFG.SchDoc	Drawn By:	



Title		
Size: A3	Number	Revision
Date: 11/05/2026	Sheet of	
File: D:\XCZU5EV_AD9361_SDR\CLOCK.SchDoc	Drawn By:	


U5B
FPGA_PART44_PL_HD
AB13 IO_L7N_HDGC_44
AA13 IO_L7P_HDGC_44
AC13 IO_L6N_HDGC_44
AC14 IO_L6P_HDGC_44
AD14 IO_L5N_HDGC_44
AD15 IO_L5P_HDGC_44
AF13 IO_L4N_AD12N_44
AE13 IO_L4P_AD12P_44
AH13 IO_L3N_AD13N_44
AG13 IO_L3P_AD13P_44
AH14 IO_L2N_AD14N_44
AG14 IO_L2P_AD14P_44
AE14 IO_L1N_AD15N_44
AE15 IO_L1P_AD15P_44
IO_L12N_AD8N_44 AA12
IO_L12P_AD8P_44 Y12
IO_L11N_AD9N_44 W11
IO_L11P_AD9P_44 W12
IO_L10N_AD10N_44 Y13
IO_L10P_AD10P_44 Y14
IO_L9N_AD11N_44 W13
IO_L9P_AD11P_44 W14
IO_L8N_HDGC_44 AB14
IO_L8P_HDGC_44 AB15
VCCO_44 AA14
VCCO_44 AD13
C385 4.7uF
C386 4.7uF
GND
VCC_3V3
U5C
FPGA_PART45_PL_HD
CLK-40M-DAC-nSYNC F11
CLK-40M-DAC-DIN F12
CLK-40M-DAC-SCLK F10
G11
H12
J12
G10
H11
K12
K13
J10
J11
IO_L6N_HDGC_45
IO_L6P_HDGC_45
IO_L5N_HDGC_45
IO_L5P_HDGC_45
IO_L4N_AD12N_45
IO_L4P_AD12P_45
IO_L3N_AD13N_45
IO_L3P_AD13P_45
IO_L2N_AD14N_45
IO_L2P_AD14P_45
IO_L1N_AD15N_45
IO_L1P_AD15P_45
IO_L12N_AD8N_45 C12
IO_L12P_AD8P_45 D12
IO_L11N_AD9N_45 A11
IO_L11P_AD9P_45 A12
IO_L10N_AD10N_45 A10
IO_L10P_AD10P_45 B11
IO_L9N_AD11N_45 B10
IO_L9P_AD11P_45 C11
IO_L8N_HDGC_45 D11
IO_L8P_HDGC_45 E12
IO_L7N_HDGC_45 D10
IO_L7P_HDGC_45 E10
VCCO_45 B12
VCCO_45 E11
C389 4.7uF
C390 4.7uF
GND
VCC_3V3
J4
PZ254V-12-12P
U5A
FPGA_PART43_PL_HD
AD12 IO_L6N_HDGC_AD6N_43
AC12 IO_L6P_HDGC_AD6P_43
AF12 IO_L5N_HDGC_AD7N_43
AE12 IO_L5P_HDGC_AD7P_43
AF10 IO_L4N_AD8N_43
AE10 IO_L4P_AD8P_43
AH11 IO_L3N_AD9N_43
AH12 IO_L3P_AD9P_43
AG11 IO_L2N_AD10N_43
AF11 IO_L2P_AD10P_43
AH10 IO_L1N_AD11N_43
AG10 IO_L1P_AD11P_43
IO_L12N_AD0N_43 AB9
IO_L12P_AD0P_43 AB10
IO_L11N_AD1N_43 AA8
IO_L11P_AD1P_43 Y9
IO_L10N_AD2N_43 Y10
IO_L10P_AD2P_43 W10
IO_L9N_AD3N_43 AA10
IO_L9P_AD3P_43 AA11
IO_L8N_HDGC_AD4N_43 AC11
IO_L8P_HDGC_AD4P_43 AB11
IO_L7N_HDGC_AD5N_43 AD10
IO_L7P_HDGC_AD5P_43 AD11
VCCO_43 AC10
VCCO_43 AG12
C387 4.7uF
C388 4.7uF
GND
VCC_3V3
U5D
FPGA_PART46_PL_HD
E13 IO_L6N_HDGC_AD6N_46
E14 IO_L6P_HDGC_AD6P_46
D14 IO_L5N_HDGC_AD7N_46
D15 IO_L5P_HDGC_AD7P_46
C13 IO_L4N_AD8N_46
C14 IO_L4P_AD8P_46
A13 IO_L3N_AD9N_46
B13 IO_L3P_AD9P_46
A14 IO_L2N_AD10N_46
B14 IO_L2P_AD10P_46
A15 IO_L1N_AD11N_46
B15 IO_L1P_AD11P_46
AUART_TX_ESP
AUART_RX_ESP
GPS_RXD
GPS_TXD
GPS_PPS
IO_L12N_AD0N_46 L13
IO_L12P_AD0P_46 L14
IO_L11N_AD1N_46 J14
IO_L11P_AD1P_46 K14
IO_L10N_AD2N_46 H13
IO_L10P_AD2P_46 H14
IO_L9N_AD3N_46 G14
IO_L9P_AD3P_46 G15
IO_L8N_HDGC_AD4N_46 E15
IO_L8P_HDGC_AD4P_46 F15
IO_L7N_HDGC_AD5N_46 F13
IO_L7P_HDGC_AD5P_46 G13
VCCO_46 C15
VCCO_46 F14
C391 4.7uF
C392 4.7uF
GND
VCC_3V3
Title
Size A3
Number
Revision
Date: 11/05/2026
File: D:\XCZU5EV_AD9361_SDR\NO USE B210\USB.SchDoc
Sheet of
Drawn By:


VREF GND TCK TDO TDI TMS
UART
NO
NO
NO
NO
WIF
GPS
RX1
RX2
TX2
12V VIN

