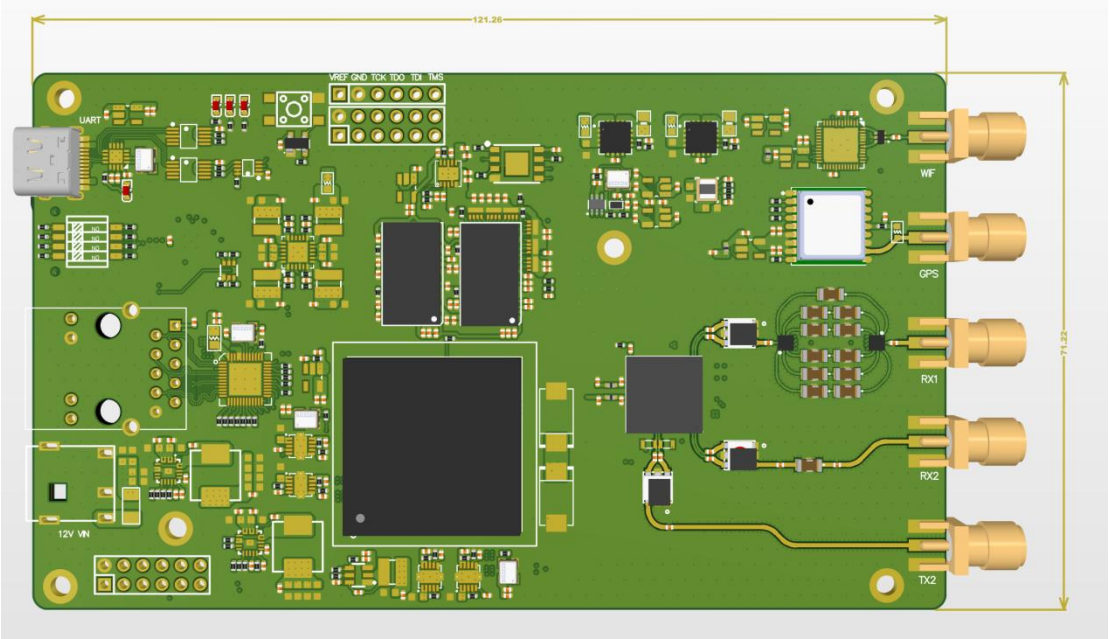
KU210 User Manual

1. Dimensions: 120mm × 70mm



2. supply electricity

DC12V 5.5*2.5mm

3.

FPGA:XCZU5EV-2SFVC784I/XCZU3EG-2SFVC784I

RFIC:AD9361

DDR4:MT40A512M16JY-083E:B *2 (2GByte)

FLASH:MT25QU256ABA1EW7-0SIT (32MByte)

ETH_PHY:RTL8211E-VL

4. peripheral

(1) Gigabit network port on the PS end

(2) Turn on the mode switch

(3) PS GPIO*11 PL GPIO*10

(4) USB-to-serial port*2, FPGA, PS, 1 channel, ESP32-C5, 1 channel

5. radio frequencySMA

(1) SMA Wi-Fi connected to ESP32-C5; supports 2.4 GHz, 5.2 GHz, and 5.8 GHz; frequency sweep/SSID

(2) GPS, BeiDou/GPS/Glonass

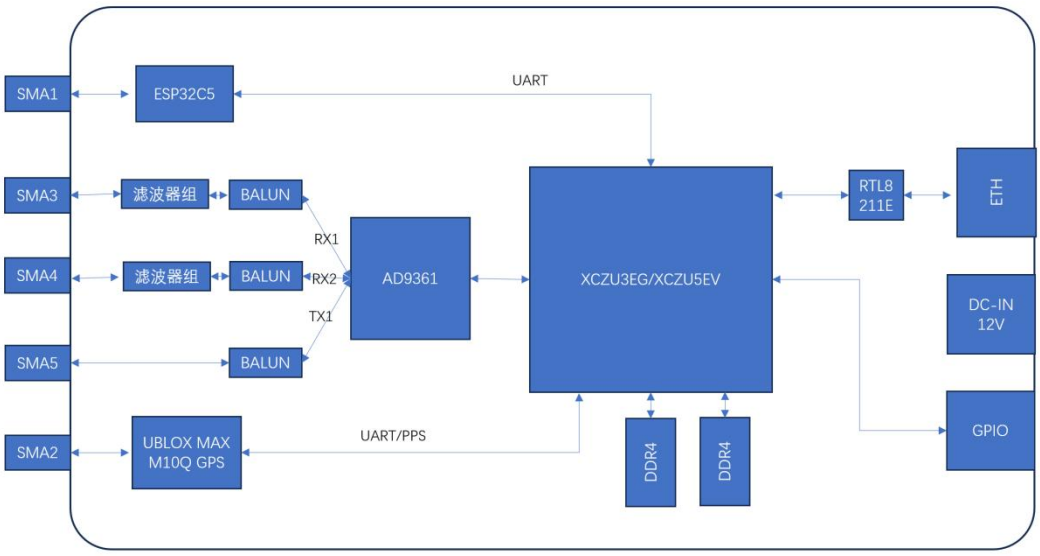
(3) RX1 SMA filter bank connected to the RX1A of the AD9361

		FRONT_V1	FRONT_V2	FRONT_V3	BACK_V1	BACK_V2	BACK_V3
<750MHz	RF5 RF6 100 101	1	0	0	1	0	1
<1700MHz	RF6 RF5 101 100	1	0	1	1	0	0
<2450MHz	RF3 RF4 010 011	0	1	0	0	1	1
<3762MHz	RF4 RF3 011 010	0	1	1	0	1	0
<5575MHz	RF1 RF2 000 001	0	0	0	0	0	1
<5850MHz	RF2 RF1 001 000	0	0	1	0	0	0

(4) The RX2 SMA filter LFCN-5850+ can be connected to the RX2A of the AD9361 at frequencies below 5850 MHz.

(5) TX2 SMA connected to the TX2A of the AD9361

6. block diagram

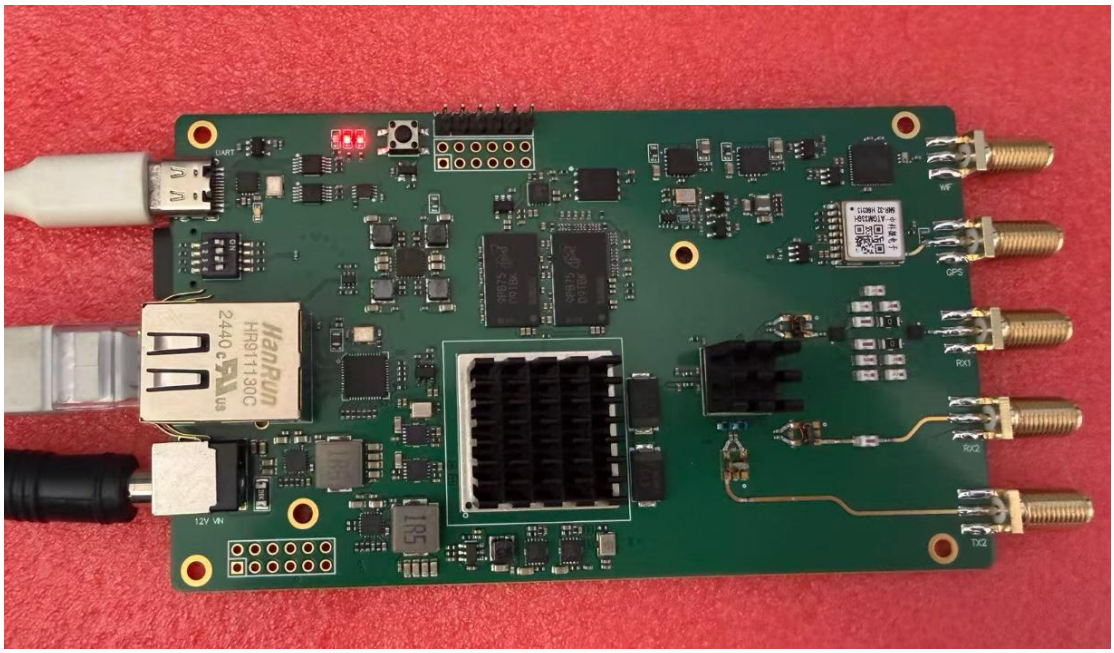


7. test

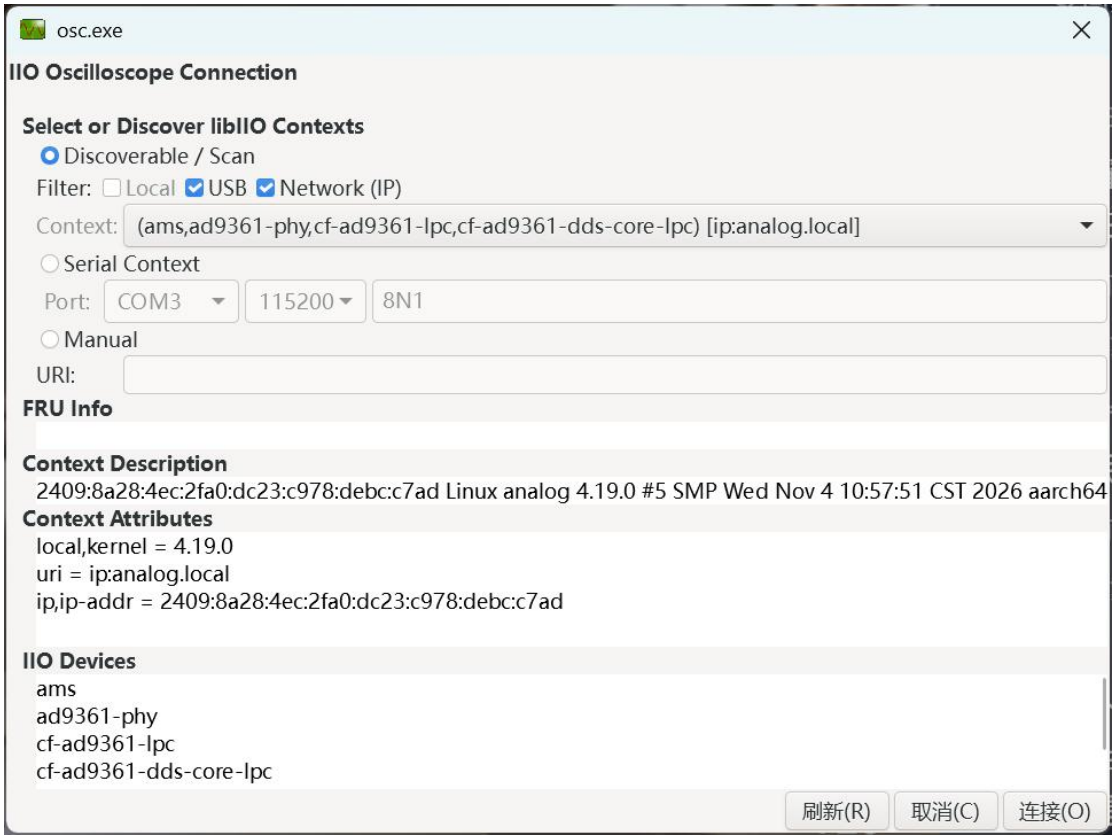
(1) Connect to the 12 V power supply

(2) Connect the network cable to the computer and set the computer's network interface IP to 192.168.1.1xx (the card's IP is 192.168.1.10).

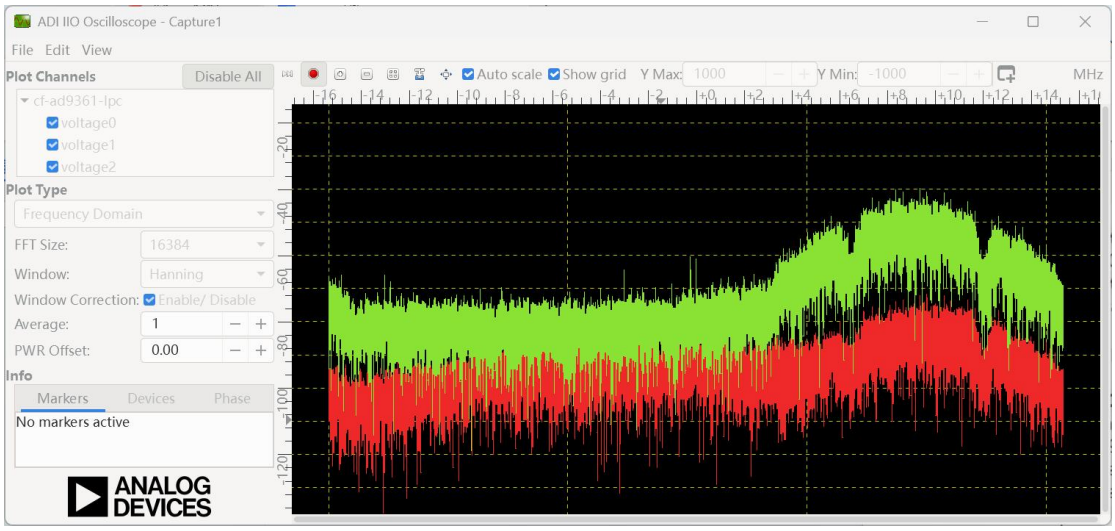
(3) TYPEC connected to the Serial Port Debug Assistant



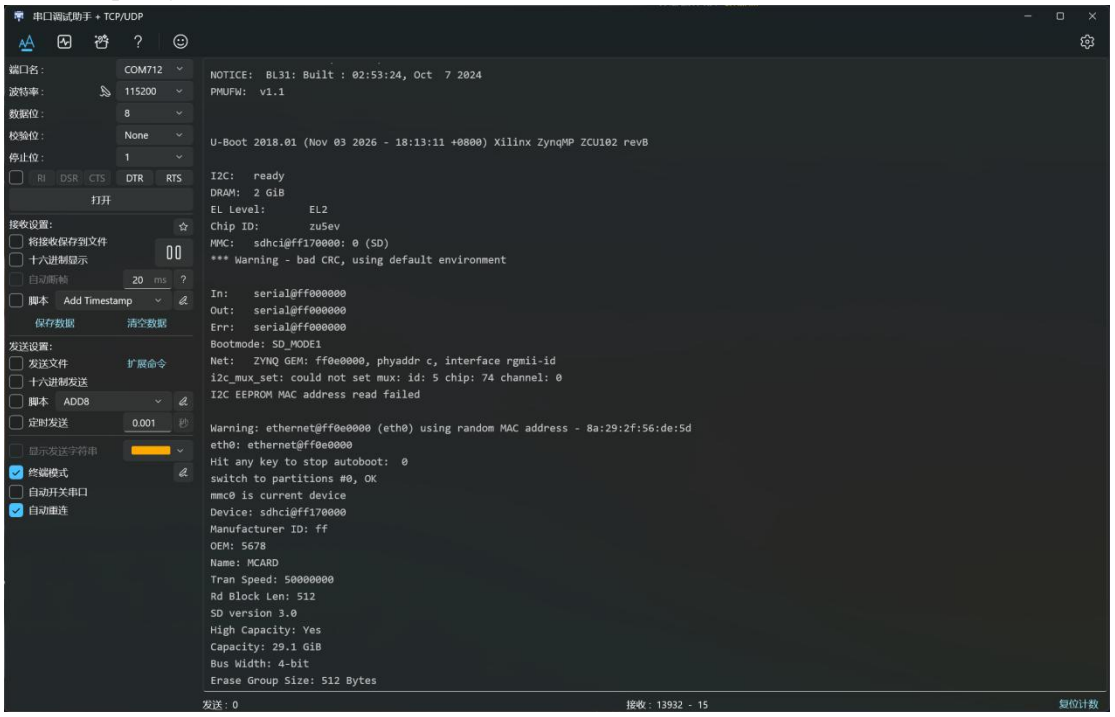
(4) Open the iio oscilloscope



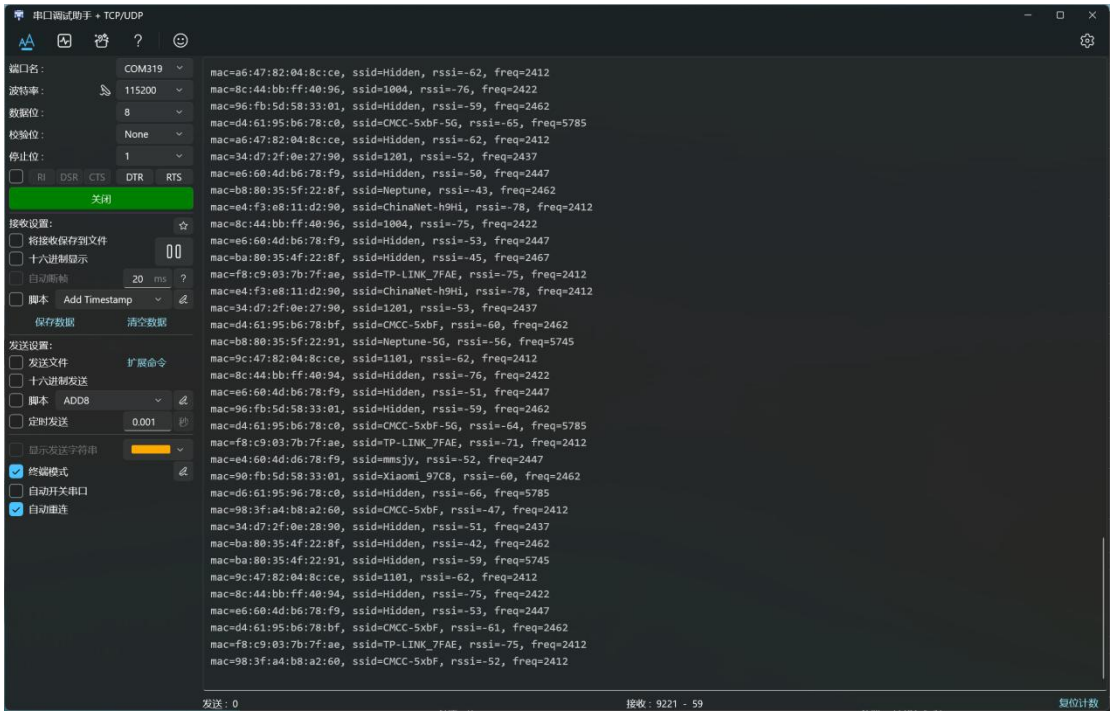
(5) Open the iio oscilloscope to acquire the spectrum



(6) Startup Log



(7) ESP Scan Log



Command for retrieving GPS information after logging in via the serial port board

```
stty -F /dev/ttyUL2 9600 cs8 -cstopb -parenb
cat /dev/ttyUL2
```

```
root@analog:/dev# stty -F /dev/ttyUL2 9600 cs8 -cstopb -parenb
root@analog:/dev# cat /dev/ttyUL2
,,,,,,,,,,,,25.5,25.5,25.5,4*04

$GPGSV,1,1,00,0*65

$BDGSV,1,1,00,0*74

$GNRMC,,V,,,,,,,,,,N,V*37

$GNVTG,,,,,,,,,N*2E

$GNZDA,,,,,,*56

$GPTXT,01,01,01,ANTENNA OPEN*25

$GNGGA,,,,,,0,00,25.5,,,,,,*64

$GNGLL,,,,,,V,N*7A

$GNGSA,A,1,,,,,,,,,,,,25.5,25.5,25.5,1*01

$GNGSA,A,1,,,,,,,,,,,,25.5,25.5,25.5,4*04

$GPGSV,1,1,00,0*65

$BDGSV,1,1,00,0*74

$GNRMC,,V,,,,,,,,,,N,V*37

$GNVTG,,,,,,,,,N*2E

$GNZDA,,,,,,*56

$GPTXT,01,01,01,ANTENNA OPEN*25
```

Command to retrieve Wi-Fi information

```
stty -F /dev/ttyUL0 115200 cs8 -cstopb -parenb
cat /dev/ttyUL0
```

```
root@analog:/dev# stty -F /dev/ttyUL0 115200 cs8 -cstopb -parenb
root@analog:/dev# cat /dev/ttyUL0
mac=34:d7:2f:0e:27:90, ssid=1201, rssi=-52, freq=2437
mac=b8:80:35:5f:22:8f, ssid=Neptune, rssi=-38, freq=2462
mac=ba:80:35:4f:22:91, ssid=Hidden, rssi=-63, freq=5745
mac=a6:47:82:04:8c:ce, ssid=Hidden, rssi=-64, freq=2412
mac=a6:47:82:04:8c:ce, ssid=Hidden, rssi=-65, freq=2417
mac=34:d7:2f:0e:27:90, ssid=1201, rssi=-54, freq=2437
mac=96:fb:5d:58:33:01, ssid=Hidden, rssi=-57, freq=2462
mac=ba:80:35:4f:22:91, ssid=Hidden, rssi=-66, freq=5745
mac=9c:47:82:04:8c:ce, ssid=1101, rssi=-66, freq=2412
mac=c8:bf:4c:73:ea:d2, ssid=Later, rssi=-79, freq=2412
mac=34:d7:2f:0e:28:90, ssid=Hidden, rssi=-54, freq=2437
mac=d4:61:95:b6:78:bf, ssid=CMCC-5xbF, rssi=-54, freq=2462
mac=d6:61:95:96:78:c0, ssid=Hidden, rssi=-68, freq=5785
mac=d4:35:38:87:9d:ec, ssid=xyjffb, rssi=-74, freq=2412
mac=8c:44:bb:ff:40:96, ssid=1004, rssi=-78, freq=2422
mac=34:d7:2f:0e:28:90, ssid=Hidden, rssi=-54, freq=2437
mac=ba:80:35:4f:22:8f, ssid=Hidden, rssi=-41, freq=2462
mac=ba:80:35:4f:22:91, ssid=Hidden, rssi=-63, freq=5745
```

Filter bank switching command

iio_attr -c ad9361-phy altvoltage0 frequency 2501000000

Switching Logic

```
// ***************************************************************************
// ***************************************************************************

// RX1A filter bank. front_v/back_v are {V3,V2,V1}, V1 is bit 0.
// SKY13418-485LF Table 4 is written V1 V2 V3:
//   RF1=000 RF2=001 RF3=010 RF4=011 RF5=100 RF6=101
// path 0 and anything else select path 1.
module rx1a_rf_gpio (
  input   wire  [2:0] path,
  output  reg   [2:0] front_v,
  output  reg   [2:0] back_v
);
  always @(*) begin
    case (path)
      3'd2: begin front_v = 3'b101; back_v = 3'b001; end
      3'd3: begin front_v = 3'b010; back_v = 3'b110; end
      3'd4: begin front_v = 3'b110; back_v = 3'b010; end
      3'd5: begin front_v = 3'b000; back_v = 3'b100; end
      3'd6: begin front_v = 3'b100; back_v = 3'b000; end
      default: begin front_v = 3'b001; back_v = 3'b101; end
    endcase
  end
endmodule
```

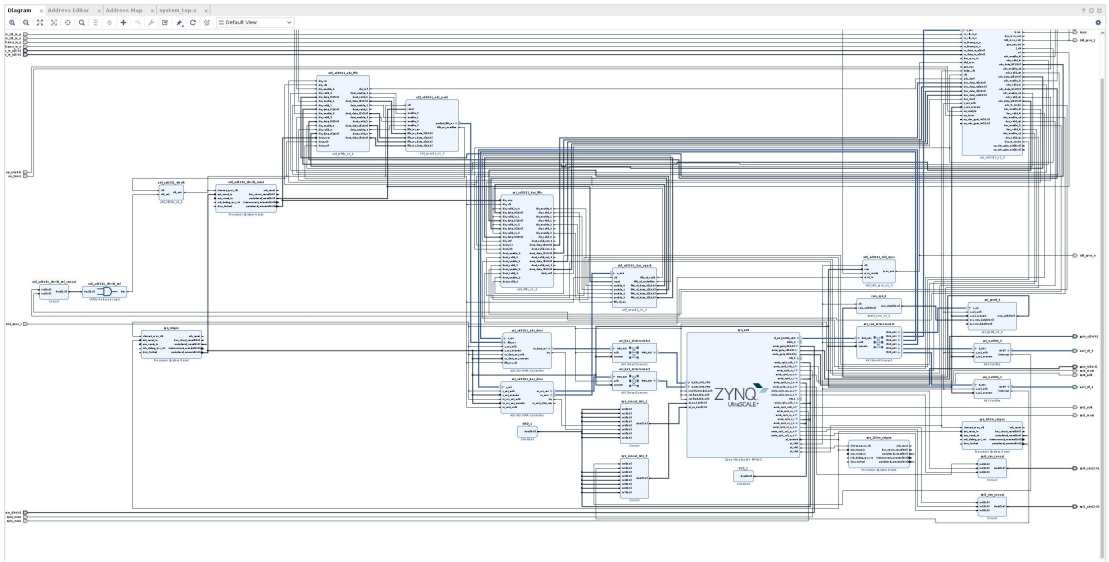
```
&adc0_ad9361 {
        en_agc-gpios = <&gpio 122 0>;
        sync-gpios = <&gpio 123 0>;
        reset-gpios = <&gpio 124 0>;
        enable-gpios = <&gpio 125 0>;
        txnrx-gpios = <&gpio 126 0>;

        /* gpio_o[11:9], bit 9 is path[0]. 0 = low, 1 = high. */
        adi,band-ctl-0-gpios = <&gpio 87 0>;
        adi,band-ctl-1-gpios = <&gpio 88 0>;
        adi,band-ctl-2-gpios = <&gpio 89 0>;

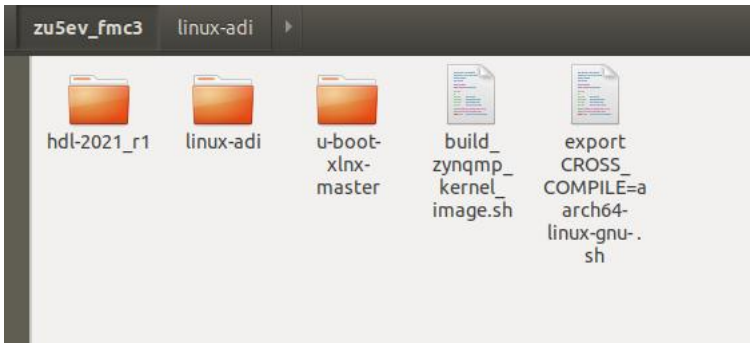
        adi_ext_band_ctl_init {
                /* 2400 MHz default LO is path 3 */
                adi,gpio-settings = <1 1 0>;
        };

        adi_rx_band_setting_0 {
                adi,lo-freq-min = /bits/ 64 <0>;
                adi,lo-freq-max = /bits/ 64 <750000000>;
                adi,gpio-settings = <1 0 0>;
        };
        adi_rx_band_setting_1 {
                adi,lo-freq-min = /bits/ 64 <750000000>;
                adi,lo-freq-max = /bits/ 64 <1700000000>;
                adi,gpio-settings = <0 1 0>;
        };
        adi_rx_band_setting_2 {
                adi,lo-freq-min = /bits/ 64 <1700000000>;
                adi,lo-freq-max = /bits/ 64 <2640000000>;
                adi,gpio-settings = <1 1 0>;
        };
        adi_rx_band_setting_3 {
                adi,lo-freq-min = /bits/ 64 <2640000000>;
                adi,lo-freq-max = /bits/ 64 <3762500000>;
                adi,gpio-settings = <0 0 1>;
        };
        adi_rx_band_setting_4 {
                adi,lo-freq-min = /bits/ 64 <3762500000>;
                adi,lo-freq-max = /bits/ 64 <5575000000>;
                adi,gpio-settings = <1 0 1>;
        };
        adi_rx_band_setting_5 {
                adi,lo-freq-min = /bits/ 64 <5575000000>;
                adi,lo-freq-max = /bits/ 64 <7000000000>;
                adi,gpio-settings = <0 1 1>;
        };
};
```

The overall block diagram has been modified based on the ZCU102_FMCOMMS2-3.



code

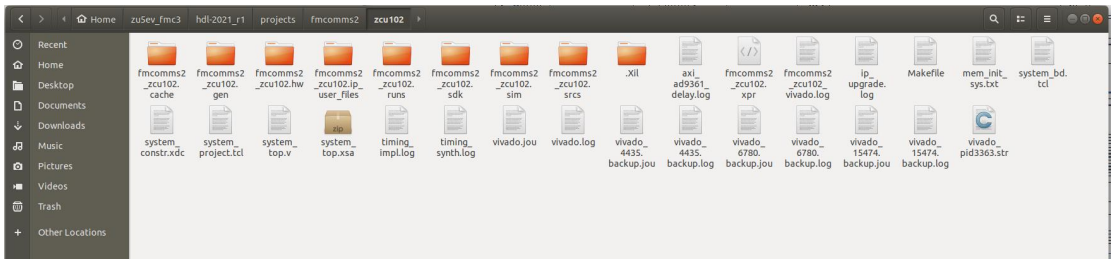


export PATH=$PATH:/tools/Xilinx/Vitis/2021.1/gnu/aarch64/lin/aarch64-linux/bin
export CROSS_COMPILE=aarch64-linux-gnu-
export ARCH=aarch64
make xilinx_zynqmp_zcu102_revB_defconfig

source /tools/Xilinx/Vivado/2021.1/settings64.sh
./build_zynqmp_boot_bin.sh system_top.xsa u-boot.elf

make adi_zynqmp_defconfig
make xilinx/zynqmp-zcu102-rev10-ad9361-fmcomms2-3.dtb

VIVADO Project Path




```
67
68 # RX1A filter switches, Bank 66. U16 = FRONT_V*, U19 = BACK_V*.
69 # V1 is bit 0 of the GPIO vector in rx1a_rf_gpio.
70 set_property -dict {PACKAGE_PIN A1 IOSTANDARD LVCMOS18} [get_ports front_v1]
71 set_property -dict {PACKAGE_PIN B1 IOSTANDARD LVCMOS18} [get_ports front_v2]
72 set_property -dict {PACKAGE_PIN C1 IOSTANDARD LVCMOS18} [get_ports front_v3]
73 set_property -dict {PACKAGE_PIN F1 IOSTANDARD LVCMOS18} [get_ports back_v1]
74 set_property -dict {PACKAGE_PIN E1 IOSTANDARD LVCMOS18} [get_ports back_v2]
75 set_property -dict {PACKAGE_PIN D1 IOSTANDARD LVCMOS18} [get_ports back_v3]
76
77
78
79 set_property -dict {PACKAGE_PIN A13 IOSTANDARD LVCMOS33} [get_ports uart_rtl_0_rxd]  //esp
80 set_property -dict {PACKAGE_PIN B13 IOSTANDARD LVCMOS33} [get_ports uart_rtl_0_txd]
81 set_property -dict {PACKAGE_PIN B14 IOSTANDARD LVCMOS33} [get_ports uart_rtl_1_rxd]  //gps
82 set_property -dict {PACKAGE_PIN A14 IOSTANDARD LVCMOS33} [get_ports uart_rtl_1_txd]
83
84 # clocks
85
```