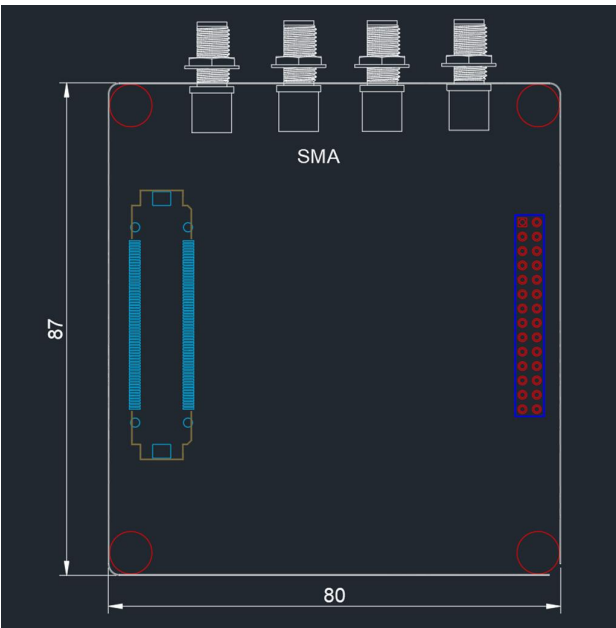


2	FPGA cell	Includes example software for FPGA hardware functional verification

4.6 System Interface Schematic



5.2 FPGA Functional Module

5.2.1 Principle Block Diagram

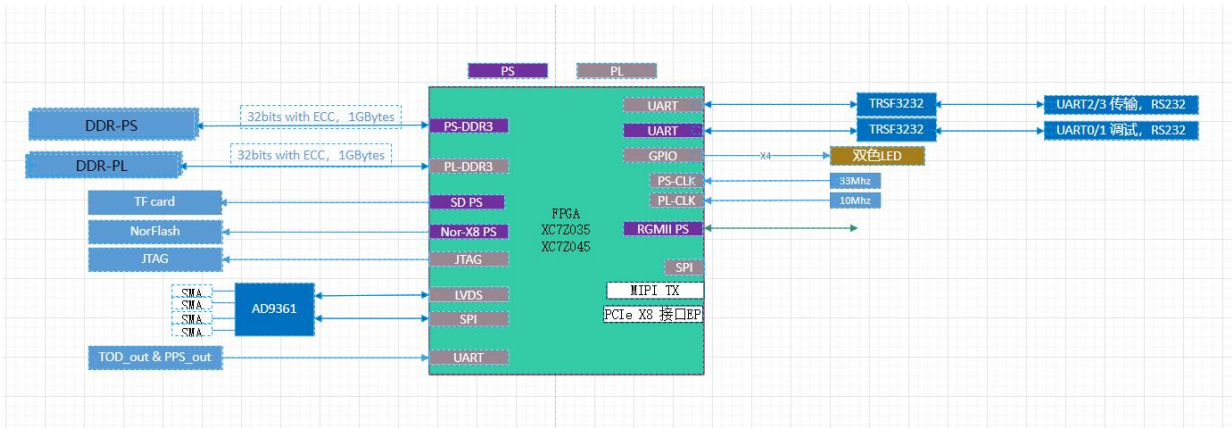


Figure 5-2: FPGA Sectional Block Diagram

5.2.2 Function List

The feature list is shown in Table 5-3.

order number	function	Signal Standard	functional description
1	DDR-1GB(PS)	DDR3	1GB RAM
2	TF CARD(PS)	TF Card	For internal use only
3	NOR FLASH(PS)		
4	Ethernet(PS)	MDI	Without transformer
5	RS232(PS)	RS232	3-pin socket
6	DDR-1GB(PL)	DDR3	1GB RAM
7	AD9361(PL)	LVDS	FPGA communication
8	TDO&PPS OUT(PL)	3.3V	Output timing data
9	PCIE X 8 EP	PCIE 2.0	ORIN Communication
10	MIPI TX	D PHY	Hardware design required; no specific software requirements.
11	SPI(PL)	indeterminate	Slave device – communicates with ORIN
12	CLK(PS)	33Mhz	
13	CLK(PL)	10Mhz	
14	GPIO(PL)	3.3V	pilot lamp
15	RS232(PL)	RS232	3-pin socket
16	JTAG		Common JTAG interface
17	power input	indeterminate	
18	antenna		4 X SMA

Table 5-3: FPGA Functional Section Interface

5.2.3 Functional Acceptance List

Functional acceptance checklist is shown in Table 5-4.

order number	function	Functional Verification Methodology	Performance Testing Methodology	remarks
1	DDR-1GB(PS)	Read/Write	Memory Read/Write Test	
2	TF CARD(PS)	Read/Write	Read/Write Speed Test	
3	NOR FLASH(PS)	Read/Write	Load firmware normally	
4	Ethernet(PS)	Supports communication	Perform speed test	
5	RS232(PS)	Supports data transmission and	No garbled text	

		reception		
6	DDR-1GB(PL)	Read/Write	Memory Read/Write Test	
7	AD9361(PL)	LVDS and SPI support communication.		
8	TDO&PPS OUT(PL)	Output timing data	The output signal is clean, without any adverse distortion.	
9	PCIE X 8 EP	Can communicate	Speed Test	
10	MIPI TX		No specific requirements	
11	SPI(PL)	Supports reading and writing data	Slave device; communicates with ORIN; clock speed exceeds 1 MHz	
12	CLK(PS)	33Mhz	Meet FPGA input requirements	
13	CLK(PL)	10Mhz	Meet FPGA input requirements	
14	GPIO(PL)	Control indicator light (on/off)	Indicator light output brightness is moderate.	
15	RS232(PL)	Supports data transmission and reception	No garbled text	
16	JTAG	Firmware flashing and debugging		
17	power input	indeterminate		
18	antenna	Strictly control impedance		

Table 5-4: FPGA Functional Component Acceptance List