

ZU_2 SD_R V01 Board Specification Sheet

1 Board Core Chip

- 1) FPGA: ZU15EG; DDR4 (PS), DDR4 (PL), QSPI Boot (128 MB);
- 2) Transceiver chip: $2 \times$ ADRV9009;
- 3) DAC chip: 1*9747;

2 Functional Performance

- 1) Supports 200 MHz bandwidth reception mode;
- 2) Supports 450 MHz bandwidth transmission mode;
- 3) Hardware supports GPIO port control for the ADRV9009-FHM functionality;
- 4) OCXO (10 MHz) or TCXO (30.72 MHz) is available as an optional option; can be selected through soldering.
- 5) Built-in fiber optic interface;
- 6) Built-in NVMe interface;
- 7) Built-in EMMC (4G).

3 Interface

- 1) Power supply requirement: Must feature a wide-voltage range design (9–32 V) with reverse-connection protection functionality;
- 2) External standard I/O interfaces shall incorporate isolation protection functionality;
- 3) The external interfaces are designed to be as close as possible to the edge of the board, facilitating subsequent installation and use.

4 Software Requirements (Provide a Bare-Metal Demo Program for MPSOC)

- 1) FPGA loading (QSPI);
- 2) Configure the ADRV9009 transceiver functionality;
- 3) Enable the AD9747 transmitter function;
- 4) Network port configuration function;
- 5) Configure DDR4 read/write operations (PS/PL);
- 6) Distribute SD card files to the PL device's DDR4,9009 for cyclic waveform playback;

5 Board Specifications:

- 1) Power input range: -50 dBm – -10 dBm;

- 2) Channel isolation:>45 dBc;
- 3) 200 MHz intra-band fluctuation: <±2 dB;
- 4) Received Signal-to-Noise Ratio (SFDR)> 50 dBc;
- 5) ADC resolution:>8.5 bits;
- 6) Maximum transmission power: for 5G networks – no less than (-15 dBm); for 3G networks – no less than (0 dBm);

6 Interface Definition

- 1) External interfaces: J30J–31J (including RS232 debugging serial port, RS485,1000 Mbps Ethernet port, RS422, power supply, etc.; the specific details shall be subject to the outcome of mutual negotiation between the parties);
- 2) Debugging interface: Features a 2.54-pin header design;
- 3) RF interface: SMP (with perforated design);
- 4) FPGA-IO Expansion: In accordance with the client's requirements, a smaller pitch of-2.54 mm is selected, and the design utilizes a 24×2 DB-9 connector;
- 5) J30J-31J Core Interface Design: The position of the interface can be appropriately adjusted; the interface specifications can subsequently be designed according to the client's requirements.

7 FPGA-IO Expansion (Adjustable, With 10 KΩ Pull-Down Resistor)

1	HR-0+	HR-0-	25
2	GND	HR-1+	26
3	HR-1-	GND	27
4	HR-2+	HR-2-	28
5	GND	HR-3+	29
6	HR-3-	GND	30
7	HR-4+	HR4-	31
8	GND	5V	32
9	GND	5V	33
10	GND	3.3V	34
11	GND	3.3V	35
12	HP-0+	HP-0-	36
13	GND	HP-1+	37
14	HP-1-	GND	38
15	HP-2+	HP-2-	39
16	GND	HP-3+	40
17	HP-3-	GND	41
18	HP-4+	HP-4-	42
19	GND	HP-5+	43
20	HP-5-	GND	44
21	HP-6+	HP-6-	45

22	GND	HP-7+	46
23	HP-7-	GND	47
24	HP-8+	HP-8-	48

